smiths interconnect

Qualification Test Report

CTX SMT Series
High Frequency Surface Mount RF Termination
Electrical and Thermal Test Report

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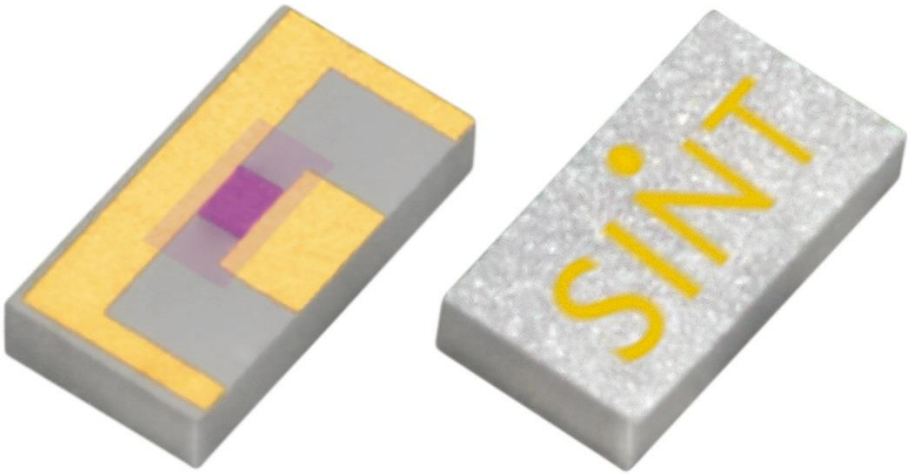
May 15, 2020
Revision 1



1. Scope

The purpose of this test report is to present the electrical and thermal performance of the high frequency surface mount termination CT0603ALN1SMTF. The report will show test data collected during the tests performed on this product. Both the pre-test simulation analysis as well as the tests on real prototypes will be displayed and analyzed. For a successful evaluation of the products at high frequencies, it is of a paramount importance for the products to be mounted on the test fixture using clearly defined mounting instructions. This report contains these mounting instructions for a future reference to be used by both the internal and external users. In addition, the test procedure is included with the test equipment used and best testing practices implemented.

Electrical performance has been evaluated through the simulation analysis and a real-life test of the DUTs in a test fixture on the vector network analyzer. Thermal performance has also been presented through a simulation and a real-life test. Thermal finite element analysis (FEA) simulations are carried out to calculate the maximum power handling of the family of parts in different environments (with different mounting constituents). The power test has been conducted in a destruct fixture that was described in the report. Finally, the set of samples has been exposed to a rigorous qualification that included Group A, Group B and Group C tests as per test plan TP-9275.

The test samples passed all the qualification test requirements. The test results that will be presented in this test report are an evidence of a successful test and viability of the product to be released into customers' applications.

2. Specifications

To cover the frequency bands of interest, a single surface mount RF termination has been designed, modeled, simulated, and tested under the part numbers CTH0603ALN1SMTF. The size of the termination is 0.060"×0.030"×0.010". These products were made using a thin film based processes on an Aluminum Nitride ceramic substrate with Tantalum Nitride resistors. Detailed specifications for the product is shown in the Tables and Figures below.

CTH0603ALN1SMTF				
ITEM	**PARAMETER**	**REQUIREMENT**	**LIMITS**	**UNITS**
1	Nominal Impedance	50 ± 10%	-	Ω
2	Frequency Range	DC – 67	-	GHz
3	VSWR	1.25:1	typical	-
4	Input Power	1.0	maximum	Watts
5	Operating Temperature	-55 to +150	-	°C
6	Non-Operating temperature	-65 to +150	-	°C

Table 1 – Electrical and Non-Electrical Requirements for CTH0603ALN1SMTF

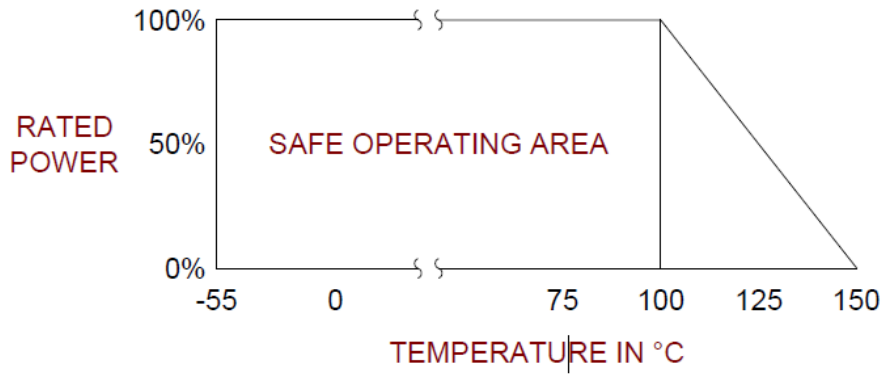


Figure 1 - Power Derating at Temperature

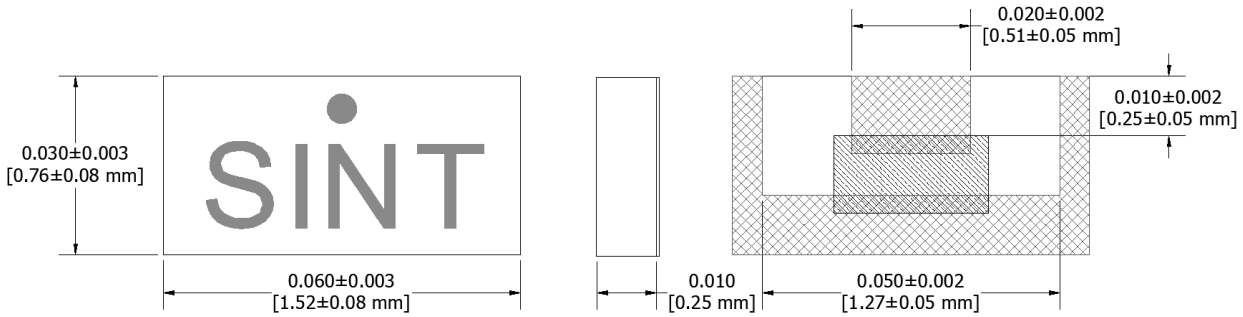


Figure 2. 2D Drawing for CTH0603ALN1SMTF - Mechanical Footprint

3. Test Preparation - Electrical (RF) Simulations

RF termination has been simulated in 3D electromagnetic simulators Ansys HFSS and Dessault CST. The purpose of the modeling in various simulation tools (Figure 3) is to compare the simulated performance and to establish the level of correlation between the simulation and the test.

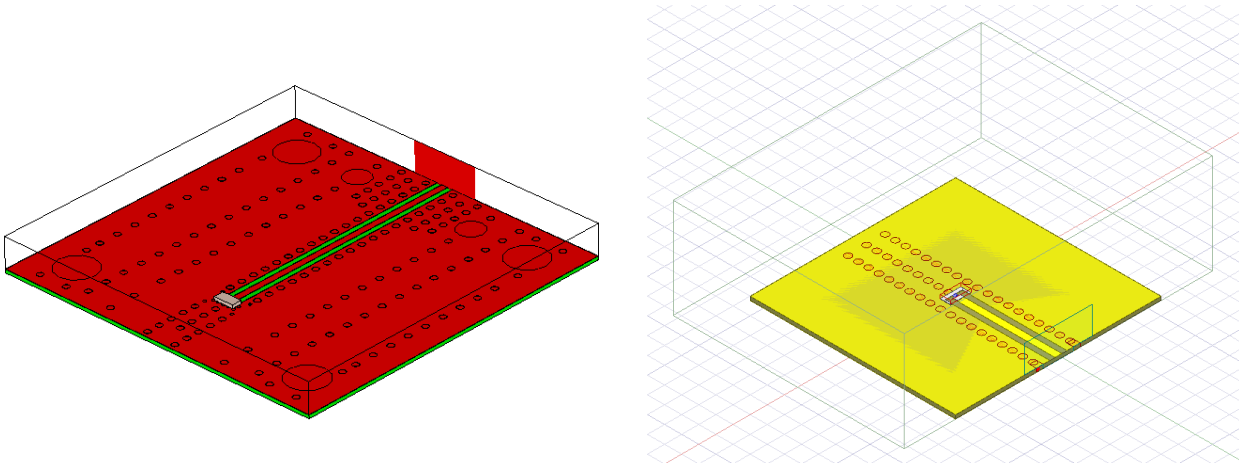


Figure 3. Electrical Models of CTH0603ALN1SMTF: (a) CST Studio, (b) HFSS

After the designs have been optimized for a nominal performance, the tolerance analysis has been conducted that considered substrate thickness and dielectric constant variations, transmission line dimensional tolerances, and variations in the bulk resistivity and shape of the resistors. Finally, the impact of the positional tolerance of the chip on the test fixture has also been evaluated in order to establish the baseline directions for the mounting of the DUT into the test fixture. Figure 4 presents the simulated electrical performance of the termination for different tolerance scenarios; as observed the termination meets the required specification.

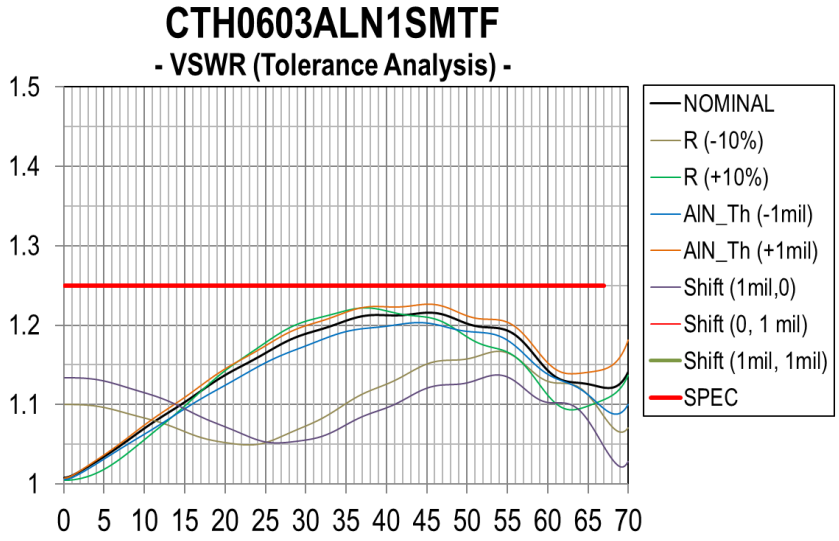
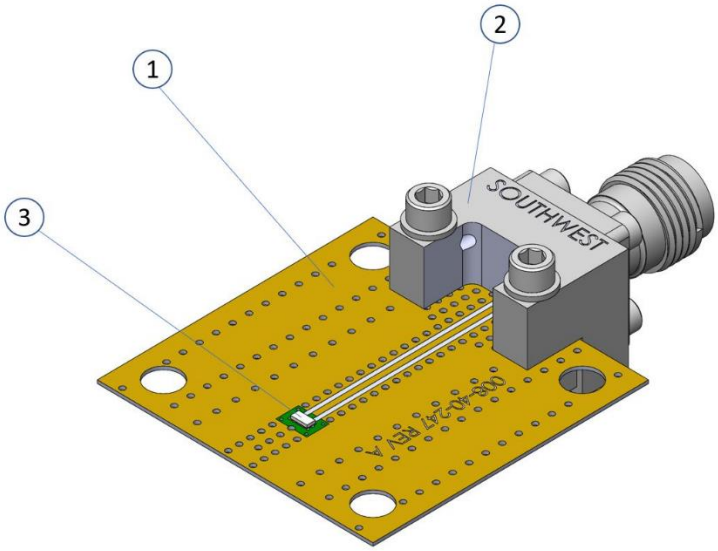
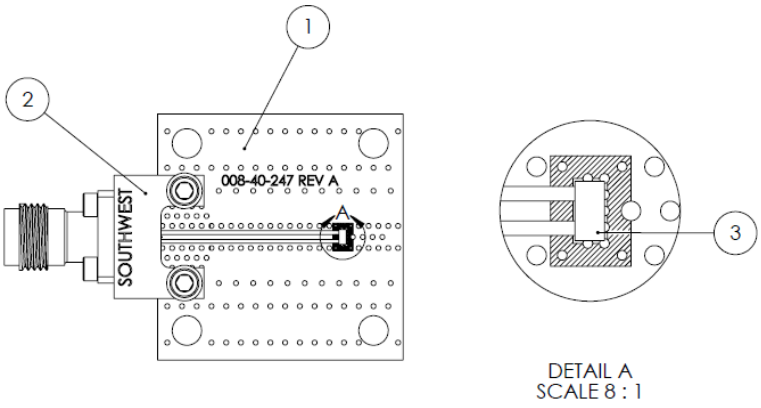


Figure 4. Simulated electrical performance for different tolerance scenarios

4. Test Fixture Choice

The test fixture (see Figure 5) that was chosen to test this product consists of a test board (Figure 6) made with Rogers 6035HTC material (0.010" thickness) and a Southwest field replaceable female end launch 1.85 mm connector (1492-06A-4). Rogers 6035HTC material has been selected due to its excellent thermal properties that would play an important role in the thermal performance of this product. It was also observed that the close proximity of the plated through via holes to the DUT improves the thermal performance of the product as it is reliant on the thermal path from the DUT via the ground bars into the test board (so called "outrigger" effect).





ITEM	ITEM NUMBER	DESCRIPTION	QTY
3	CTH0603ALN1SMTF	DUT	1
2	1892-04A-6	SOUTHWEST MICROWAVE END LAUNCH CONNECTOR (1.85mm)	1
1	008-40-247	TEST BOARD, HIGH FREQUENCY SMT RF TERMINATION	1

Figure 5. Test Fixture used to test Developed Prototypes.

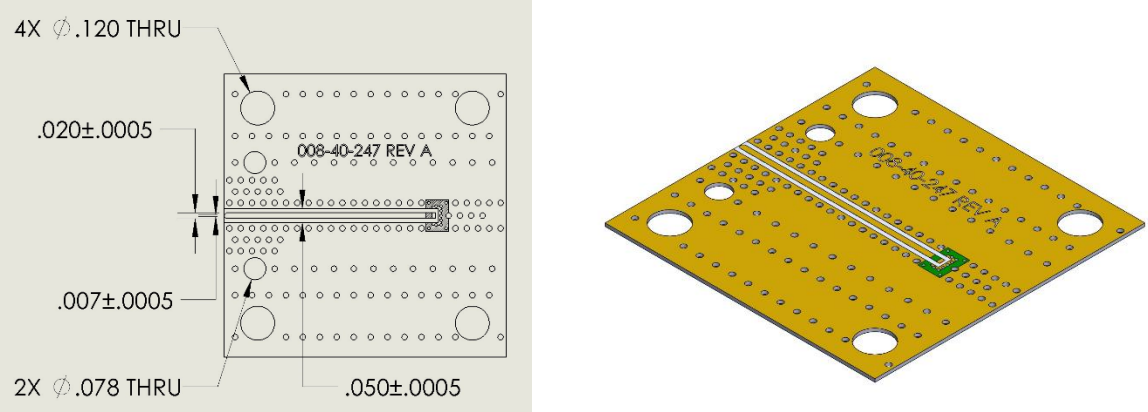


Figure 6. Test board used to interface the DUT with the connector

The 1.85 mm jack (female) end launch connector used for the tests at frequencies DC – 67 GHz is shown in Figure 7. It is important to mention that the selection of the connector pin (see dimensions ϕA) on the connector affects the connector launch performance and thus must be chosen as directed.

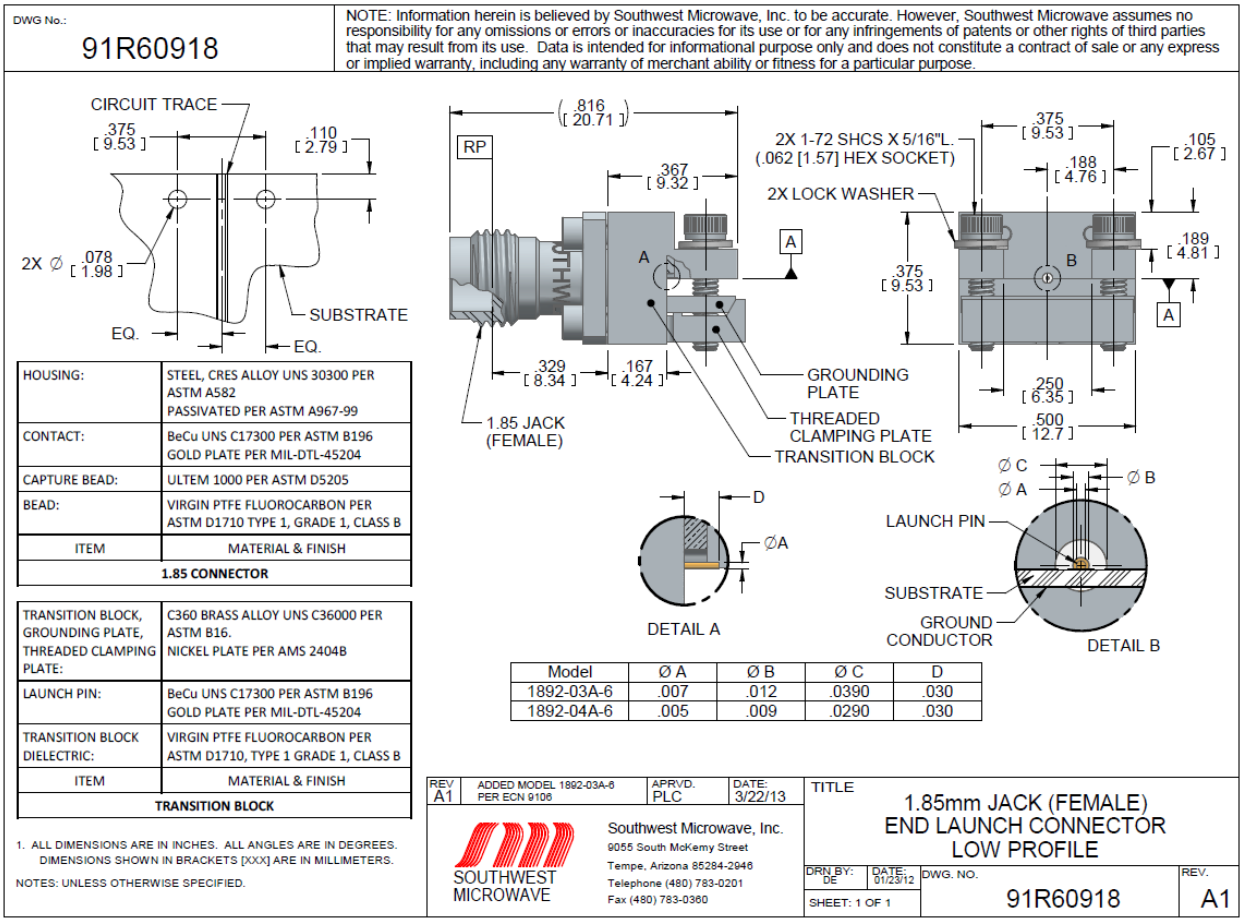


Figure 7. Southwest Microwave 1.85 mm connector used in tests at frequencies DC-67 GHz - drawing

5. Mounting Instructions

First step in properly mounting this high frequency surface mount RF termination for testing is to carefully inspect all the components of the test fixture to be assembled. Special attention should be given to the test board edges (Figure 8a). Common PCB manufacturing often leave rough edges that can cause fixture assembly issues. The edges of the test board can usually be cleaned up using fine grit sandpaper. (Figure 8b).

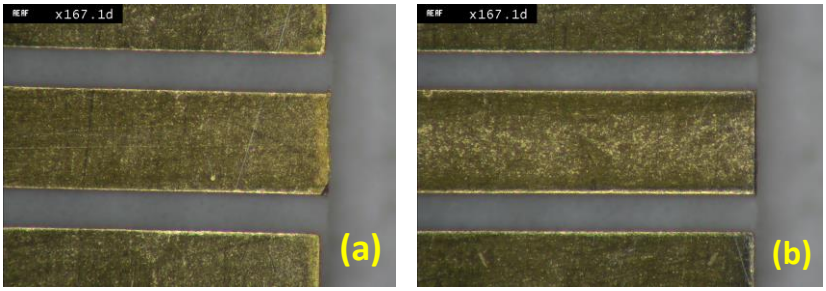


Figure 8. Test board transmission line:
(a) rough edge (before cleaning), (b) smooth edge (after cleaning)

The chip termination (DUT) should also be inspected to ensure the edges are cleanly cut and have no jagged edges prior to being installed on the test board. To avoid any potential electrical failures, the chip termination needs to be properly positioned (centered) and soldered in place. Introduction of the solder mask around the footprint area where the termination is to be soldered helps this positional alignment. The chip termination is soldered onto the test board using Sn96 solder. Care should be taken to insure there is no solder run-out into the area where the DUT is to be mounted.
The final step in the fixture assembly is to mount the connector to the test board. Things to look for at this step is to center the connector pin on the transmission line and to ensure the connector is flush with the edge of the test board to avoid undesired air gaps (Figure 9). Use of a microscope is essential to ensuring that the connector is mounted properly.

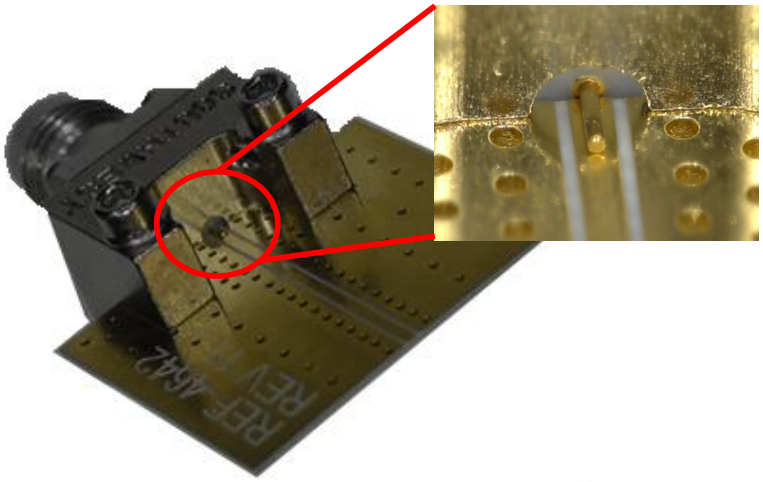


Figure 9. Connector pin alignment on the test board

The mounting instructions are shown on the block diagram (Figure 10). The fully assembled test fixture (Figure 11) consists of the test board with the DUT installed using proper mounting practices described above. The Southwest microwave connector is seen on each side of the fixture.

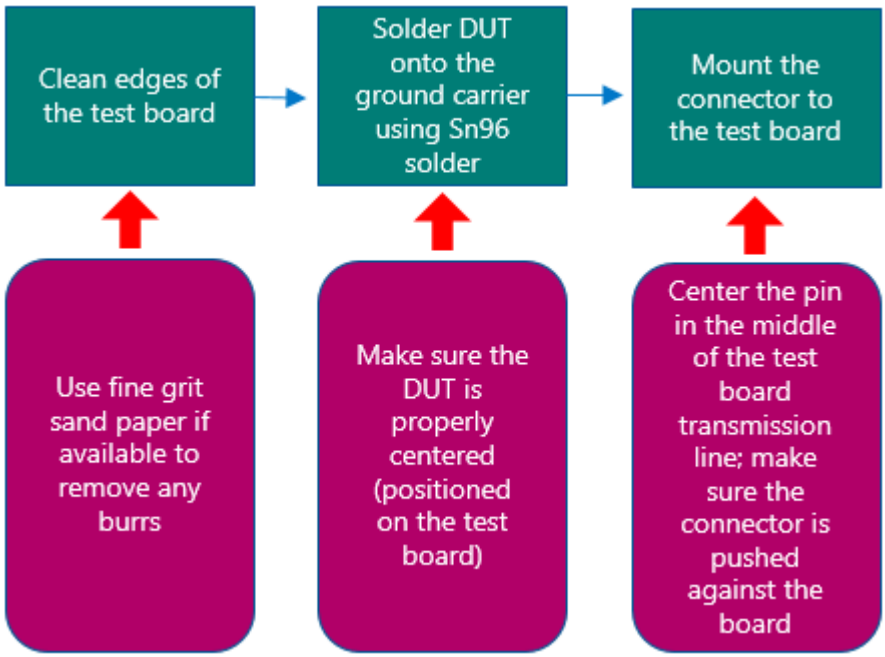


Figure 10. The Mounting instructions – Flow Chart

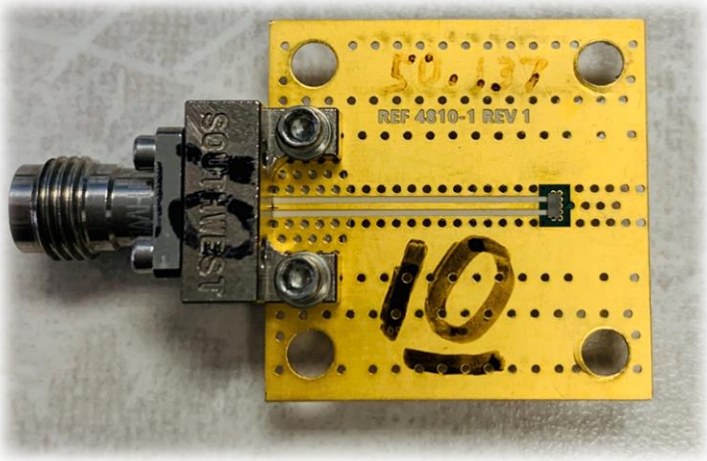
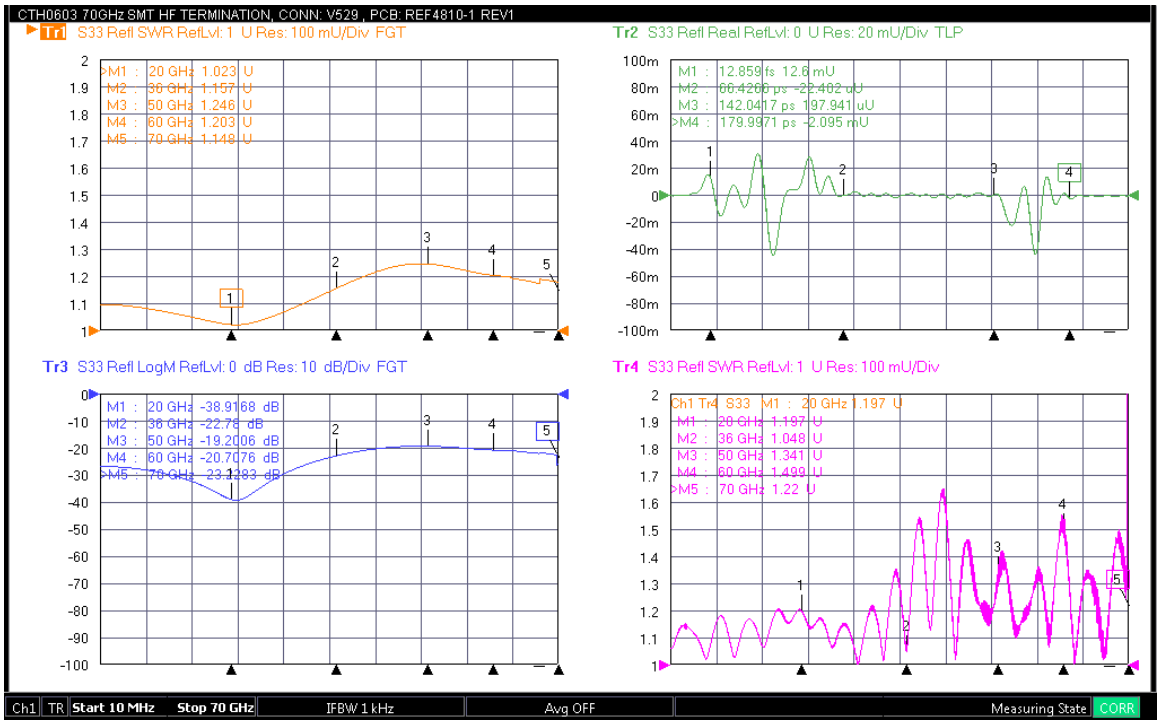


Figure 11. Fully assembled test fixture for the test of the high frequency SMT RF termination CTH0603ALN1AMTF

6. RF Test Results

Typical performance of CTH0603ALN1SMTF is shown in Figure 12. Both gated (termination only), and non-gated (termination and connector), and time-domain data is shown. The prototypes exhibit a very repetitive VSWR performance under 1.30:1 for the entire frequency band DC-67 GHz.

SAMPLE 1



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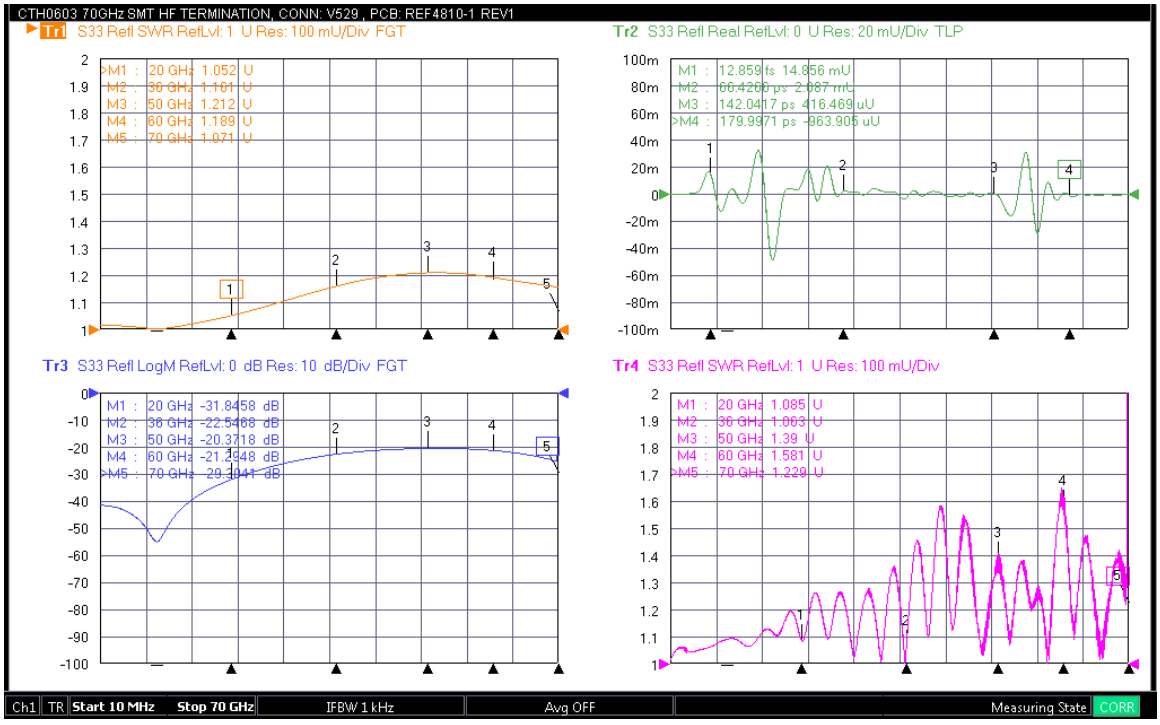

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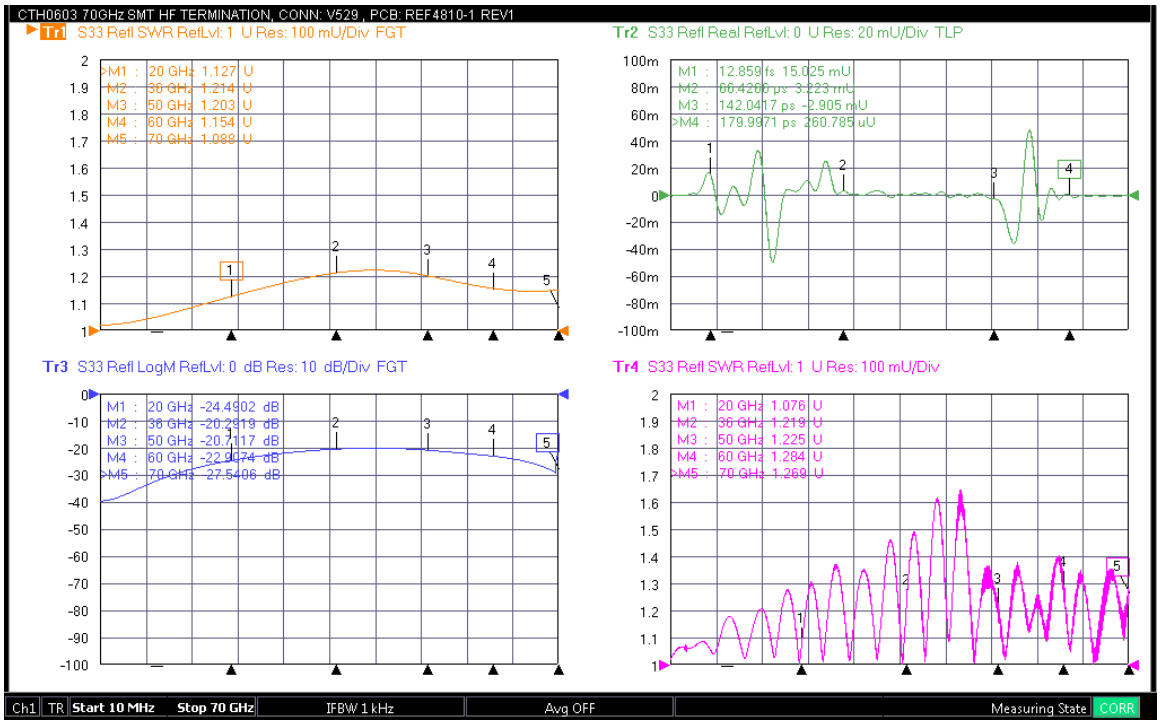


SAMPLE 4

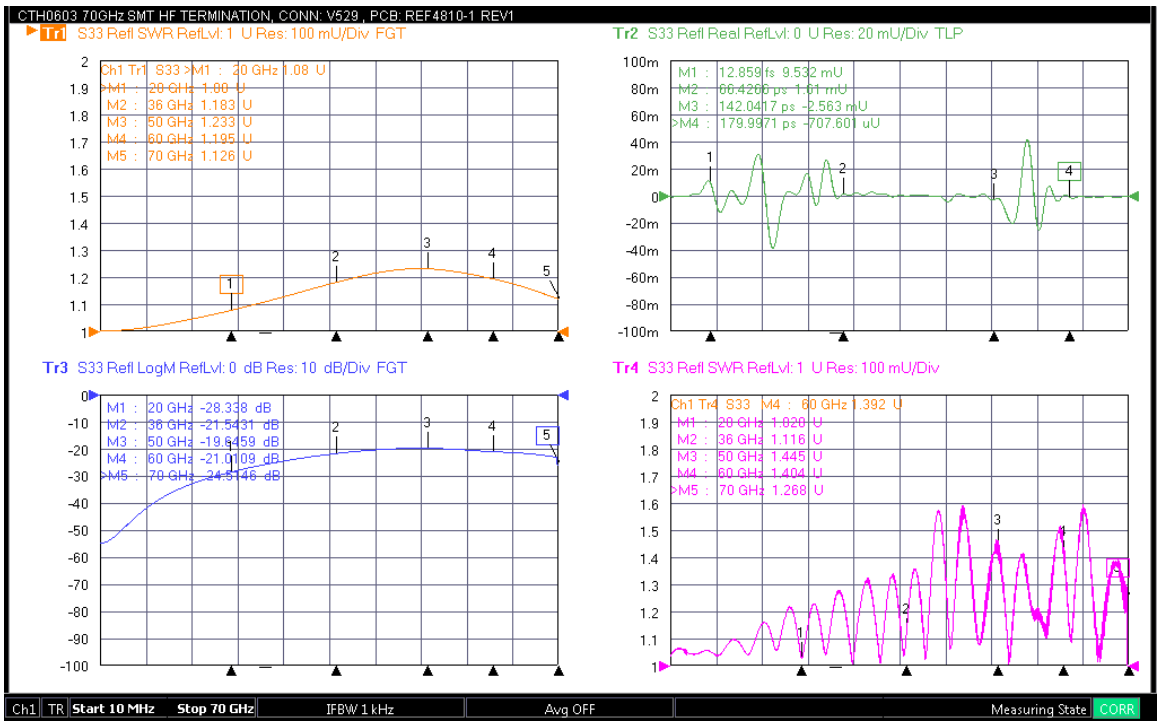
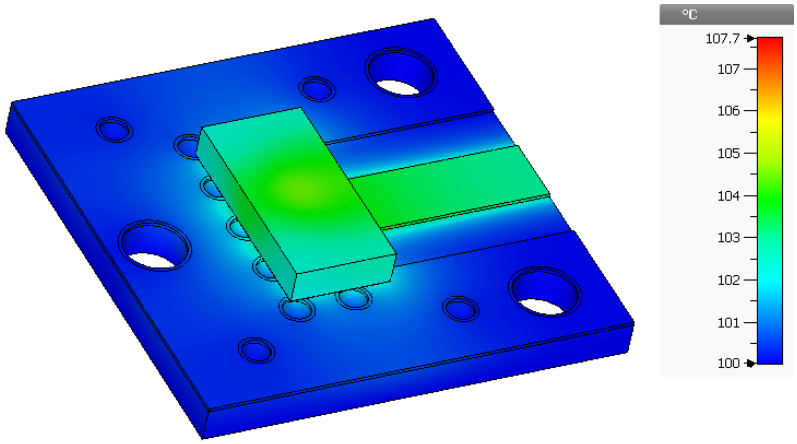


Figure 12. Typical RF performance of CTH0603ALN1SMTF termination: VSWR gated (top left), return loss gated (bottom left), time domain (top right), VSWR ungated (bottom right)

7. Thermal (FEA) Simulation

Thermal FEA simulation has been performed on this high frequency SMT RF termination using CST MPHYSICS® STUDIO. CST MPHYSICS® STUDIO (CST MPS) is a powerful and easy-to-use tool for thermal and mechanical stress analysis. High-frequency fields, currents and particle collisions are all sources of heat that EM engineers frequently encounter, and so CST MPS is fully integrated into CST STUDIO SUITE® to enable coupled EM-multiphysics simulation with other tools such as CST MICROWAVE STUDIO®, CST EM STUDIO® and CST PARTICLE STUDIO®. With the CST MPS thermal solver, the changes in temperature generated by these interactions are modeled, and heat flow within the device simulated to test the performance of heat sinks and ensure the reliability of temperature-sensitive components. From the temperature distribution, CST MPS® can also calculate the thermal expansion of the components and the stress and strain within it as it presses against its housing, using the mechanical solver. The results of the thermal expansion simulation can even be fed back into the EM simulations, offering the opportunity to perform a sensitivity analysis of the device's response to heating.

For the thermal simulation in CST MPHYSICS® STUDIO, the baseplate temperature used in the simulation was 100°C. This boundary condition was assigned to the bottom of the RF termination. All losses including losses in dielectrics and conductors were taken into account; losses from RF simulation were exported into the thermal modeler and used to properly simulate thermal flow through the structure. The film temperature of 150°C is chosen as a conservative design point to avoid resistance drift due to thermal coefficient of resistivity. Significantly higher film temperature can lead to a drift in resistance and change in attenuation. The simulation showed a delta of just 8°C on the film resistor relative to the baseplate at the input RF power levels of 1W (Figure 13). This is a significant margin that the device is expected to exhibit in the real-life test.



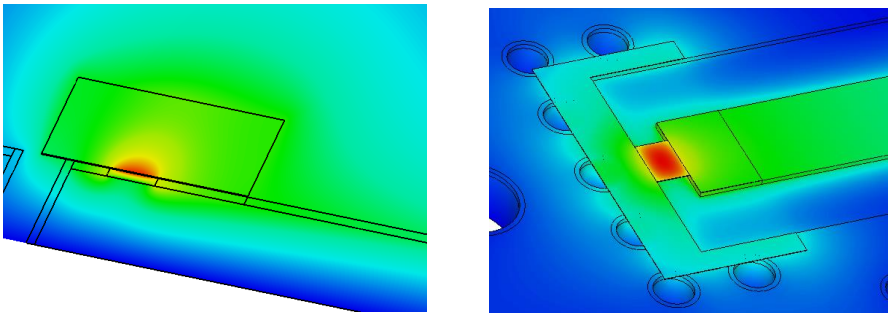


Figure 13. Simulated thermal performance of STH0603ALN1SMTF in CST MPHYSICS® Studio

It is important to mention that the true power rating of the RF chip termination in the assembly will depend on the real heatsink material for the chip mounting. There will be differences in power handling depending whether the material is a high thermal conductive metal or a poor thermal conductivity PCB material.

8. Initial Power Test

The DUT was soldered to the PCB using SN 96 solder. The PCB was then soldered to the Heatsink using SN63 (Figure 14). A type "K" thermal couple was mounted on the top surface of the DUT to monitor the device temperature. An input power of 1 W at DC was then applied for 24 hours through the RF connector. Temperature on the top side of device never exceeded 50°C. The resistance showed good stability throughout the entire test. No mechanical changes have been observed through the visual inspection of the DUT after the test was performed.

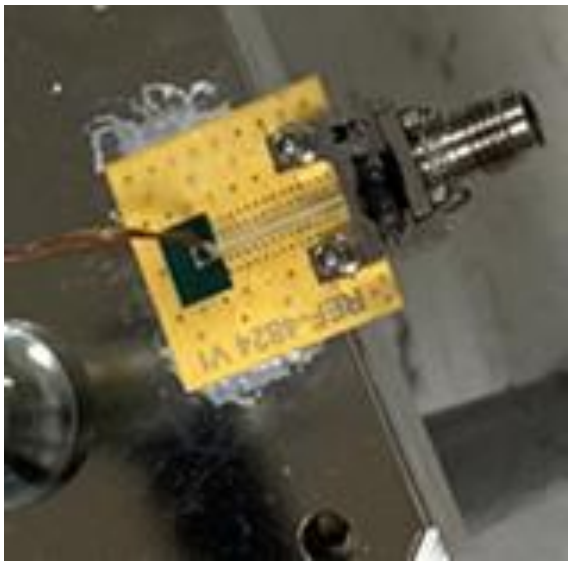


Figure 14. Test fixture used for the power handling test of the high frequency SMT RF termination

9. Qualification Test

The purpose of this test is to subject the high frequency SMT RF termination to the conditions as specified in the test plan TP-9275 and qualify this product internally for the markets to be served. The Specification Control Drawing (SCD, see Table 1) of the device was the governing document for all specification limits for each test, with any exceptions noted in the test plan. Qualification testing references MIL-PRF-55342, for Class L devices, with the exceptions noted in the test plan.

Devices were mounted on destruct fixturing in order to facilitate performance of the required tests. Removable RF connectors were be mounted only when RF test is called out. The test frequencies observed throughout the test were 20 GHz, 36 GHz, 50 GHz, 60 GHz, 67 GHz, and 70 GHz, although VSWR plots of the entire frequency band DC-67 GHz were provided.

Change in resistance incurred by tests performed was noted (if any) and used for the specification risk assessment and the final device rating. All electrical tests were conducted at DC as power handling is the main concern for the qualification. RF performance was verified at the end of each test group.

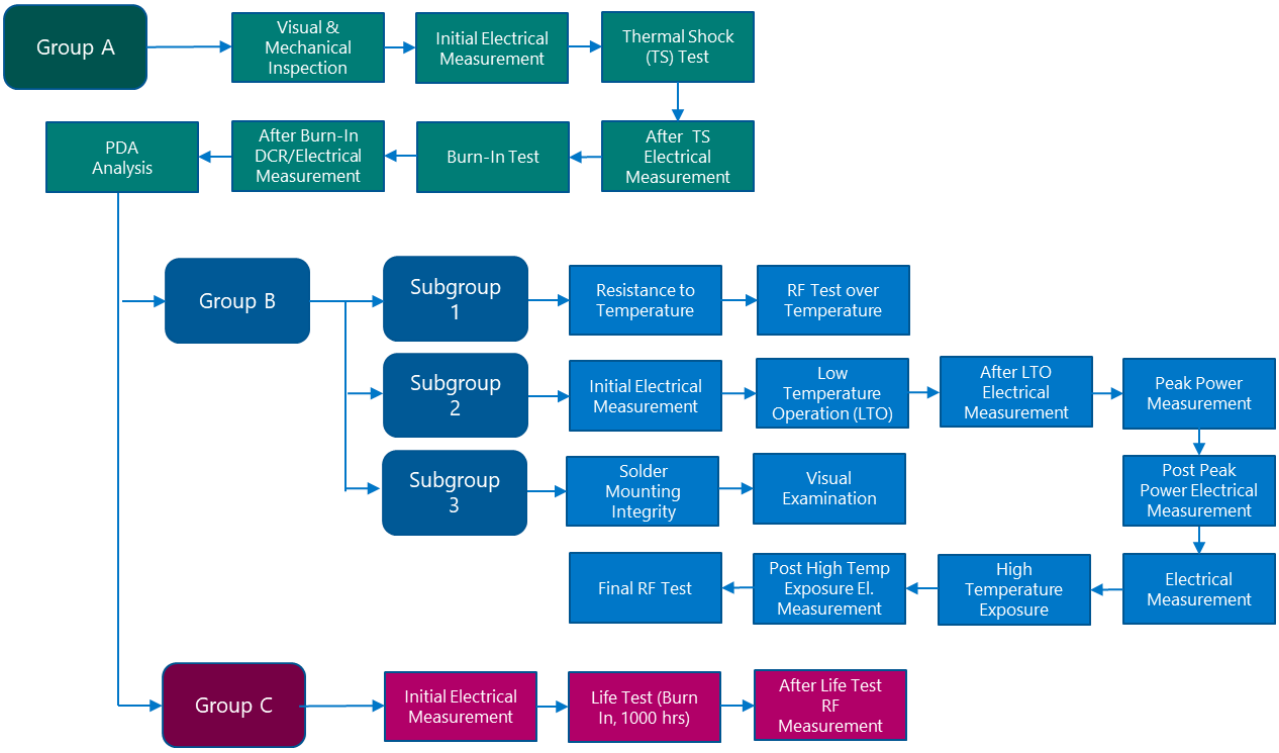


Figure 15. Flowchart of Test Procedure

GROUP A INSPECTION (100% of the lot, 20 samples)

Each inspection lot was subjected to 100% Group A inspection. The inspection lot devices were mounted onto a PCB/test fixture prior to Electrical Inspection.

Visual Mechanical Inspection Results

The materials, design, construction, physical dimensions, markings and workmanship were verified to be in accordance with applicable requirements per the appropriate SCD.

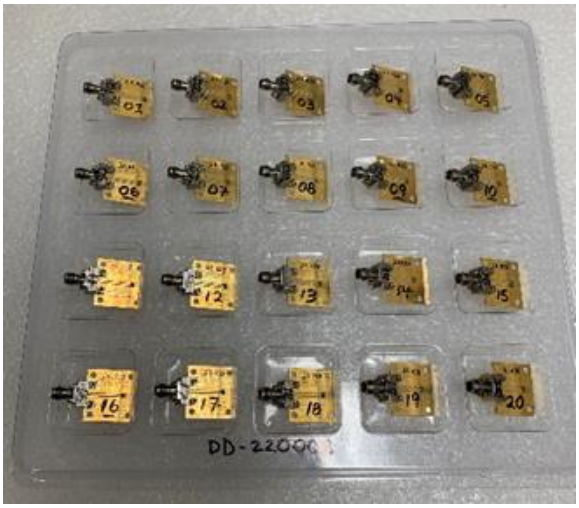


Figure 16. Group A inspection lot: test fixtures without the connectors installed (left), test fixture with the connectors installed (right)

Initial Electrical (INI) Test Results

DC resistance between the input port and the ground path (Figure 17) was measured and recorded in accordance with MIL-STD-202, Method 303. Acceptance limits were as per the SCD.
VSWR (or Return Loss) has then been measured and recorded at selected frequency points on a Vector Network Analyzer (VNA), in accordance with MIL-STD-39030, Method 4.6.10. S-parameter file for each device has been captured. Acceptance limits were as per the SCD. As indicated in Table 5, the inspection lot passed the required specification as per SCD.

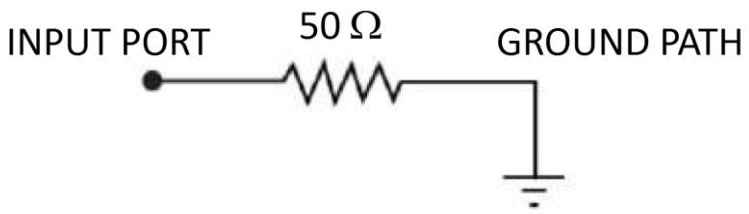


Figure 17. DC resistance test schematic diagram

HF Series Terminations per Test Plan TP-9275

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Test Group	A	Part Number	CTH0603ALN3SMTF
Test Sequence	A2	Description	70GHz HF Termination, SMT
Test Step	Initial Electrical (DC & RF) Inspection	Revision	-
Quantity	20	Test Plan	TP-9275
Date In	3/19/2020	Factory Order	REF 4796
Date Out	3/19/2020	Lot Code	16522
Operator	JA/MK	Results	Pass

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
VSWR Limit	1.50	:1

	Initial Measurements				
Serial Number	DC Resistance (Ω)	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 67 GHz
1	50.82	1.03	1.05	1.14	1.13
2	50.87	1.02	1.07	1.18	1.09
3	50.87	1.02	1.07	1.18	1.15
4	50.92	1.05	1.06	1.14	1.06
5	50.98	1.05	1.03	1.14	1.12
6	50.85	1.05	1.04	1.13	1.08
7	50.77	1.03	1.04	1.16	1.16
8	50.91	1.05	1.03	1.14	1.17
9	51.08	1.01	1.08	1.17	1.05
10	50.14	1.06	1.03	1.12	1.10
11	50.84	1.03	1.04	1.16	1.16
12	49.67	1.03	1.04	1.15	1.08
13	50.75	1.03	1.05	1.17	1.13
14	50.93	1.02	1.05	1.15	1.12
15	50.89	1.05	1.04	1.14	1.13
16	50.65	1.01	1.07	1.18	1.11
17	50.08	1.02	1.05	1.18	1.08
18	50.79	1.05	1.02	1.14	1.14
19	51.08	1.05	1.02	1.13	1.13
20	51.08	1.04	1.06	1.13	1.07

Table 2. Group A Initial Electrical Test Results - Summary

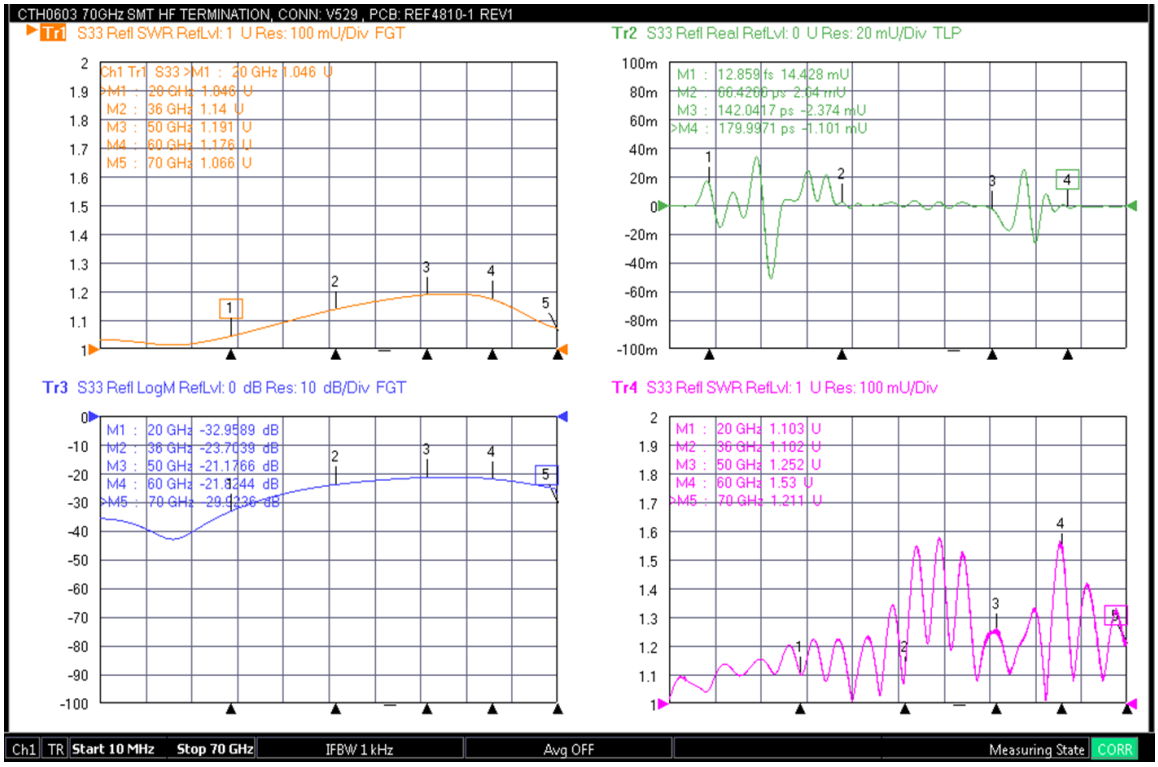

Figure 18. Group A Initial Electrical Test Results – RF performance of a typical sample from the inspection lot: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

Thermal Shock

The inspection lot samples were exposed to 10 cycles of thermal shock, -55°C to +125°C in accordance with MIL-STD-202, Method 107 (see Table 3). The equipment used for the test consisted of Thermotron, model ATS-30-4-4 with the asset tag # TE90075.

STEP	TEMPERATURE (ºC)	TIME (MINUTES)
1	-55 (+0/-3)	15 min.
2	+25 (+10/-5)	5.0 max.
3	+125 (+3/-0)	15 min.
4	+25 (+10/-5)	5.0 max.

Table 3. Thermal Shock temperature levels and exposure times

After Thermal Shock Electrical (ATS) Test Results

DC resistance between the input port and the ground path (Figure 17) was measured and recorded in accordance with MIL-STD-202, Method 303. Acceptance limits were as per the SCD and DCR Δ ±0.5 % from initial electrical. As indicated in Table 7, the inspection lot samples passed the requirements.

HF Series Terminations per Test Plan TP-9275

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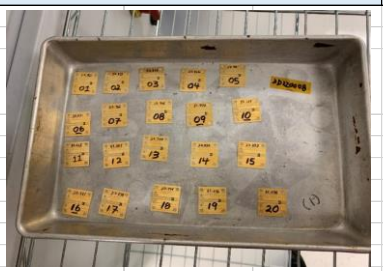
Test Group	A	Part Number	CTH0603ALN3SMTF
Test Sequence	A4	Description	70GHz HF Termination, SMT
Test Step	Post Thermal Shock Electrical (DC) Inspection	Revision	-
Quantity	20	Test Plan	TP-9275
Date In	3/20/2020	Factory Order	REF 4796
Date Out	3/20/2020	Lot Code	16522
Operator	JA/MK	Results	Pass



Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	0.5	% (±)
VSWR Limit	1.50	:1

	After Thermal Shock Measurements						Initial
Serial Number	DC Resistance (Ω)	Δ DCR (%)	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 67 GHz	DC Resistance (Ω)
1	50.83	0.01	1.04	1.04	1.13	1.12	50.82
2	50.89	0.03	1.03	1.06	1.17	1.10	50.87
3	50.89	0.03	1.03	1.06	1.17	1.14	50.87
4	50.94	0.03	1.05	1.06	1.13	1.09	50.92
5	51.01	0.05	1.05	1.03	1.14	1.13	50.98
6	50.85	0.00	1.05	1.03	1.13	1.11	50.85
7	50.79	0.05	1.03	1.04	1.15	1.11	50.77
8	50.92	0.03	1.05	1.03	1.15	1.20	50.91
9	51.08	0.01	1.01	1.08	1.17	1.14	51.08
10	50.15	0.02	1.07	1.01	1.11	1.12	50.14
11	50.84	0.02	1.03	1.04	1.16	1.15	50.84
12	49.66	-0.01	1.03	1.04	1.14	1.15	49.67
13	50.75	0.00	1.03	1.05	1.16	1.16	50.75
14	50.94	0.02	1.02	1.05	1.15	1.11	50.93
15	50.89	0.01	1.05	1.03	1.14	1.17	50.89
16	50.68	0.06	1.01	1.07	1.18	1.18	50.65
17	50.11	0.06	1.02	1.05	1.18	1.12	50.08
18	50.79	-0.01	1.06	1.01	1.16	1.18	50.79
19	51.07	-0.01	1.05	1.03	1.13	1.14	51.08
20	51.08	0.01	1.04	1.06	1.13	1.10	51.08

Table 4. Group A Post Thermal Shock Electrical Inspection Results

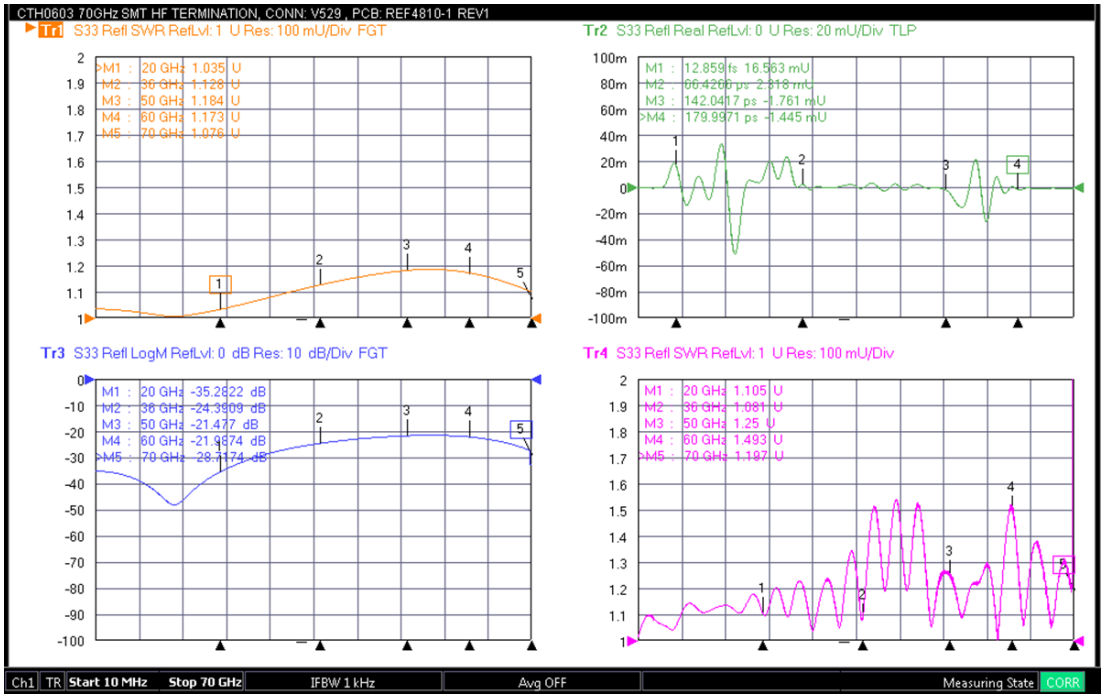
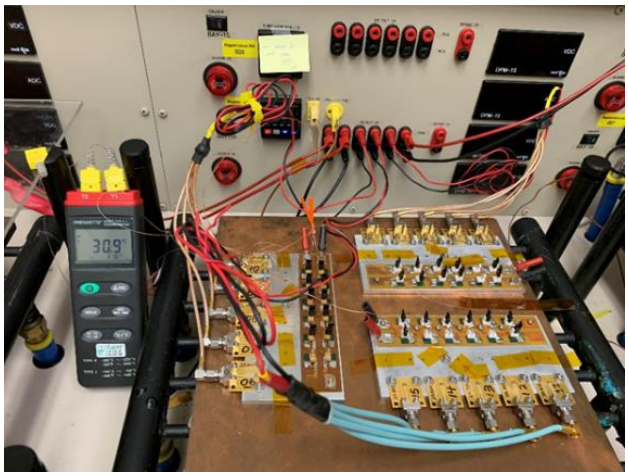


Figure 19. RF performance of a typical sample from the inspection lot after the thermal shock: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

Bake (100% de-rated burn-in)

The devices (15 samples, 75% of the lot) were to a 168-hour burn-in with a DC equivalent power as per SCD (1 W). The devices were mounted on a chilled heatsink, after which the power was turned on for a duration of 168 hours. The temperature was periodically monitored to ensure the test is not disrupted (see Figure 20). Due to the nature of the design, the film temperature couldn't be measured using a thermocouple; external device temperature was monitored to note relative changes, if they occur. After 168 hours the parts were removed from the heatsink and allowed to stabilize at room temperature for about an hour.



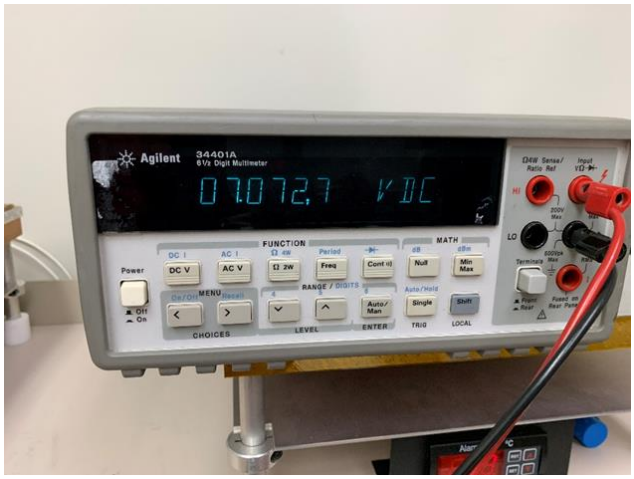


Figure 20. Burn-in test fixture

After Burn-in Electrical Test Results

DC resistance between the input port and the ground path (Figure 17) was measured and recorded in accordance with MIL-STD-202, Method 303. Acceptance limits were as per the SCD and DCR Δ ±0.5 % from after the thermal shock electrical.
VSWR (or Return Loss) has then been measured and recorded at low, mid and high frequencies on a Vector Network Analyzer (VNA), in accordance with MIL-STD-39030, Method 4.6.10. S-parameter file for each device has been captured. Acceptance limits were as per the SCD.
As shown in Table 8, the inspection lot samples passed the requirements.

HF Series Terminations per Test Plan TP-9275

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Test Group	A	Part Number	CTH0603ALN3SMTF
Test Sequence	A6	Description	70GHz HF Termination, SMT
Test Step	Post Burn In Electrical (DC & RF) Inspection	Revision	-
Quantity	15	Test Plan	TP-9275
Date In	3/30/2020	Factory Order	REF 4796
Date Out	3/30/2020	Lot Code	16522
Operator	JA/MK	Results	Pass

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	1.0	% (±)
VSWR Limit	1.30	:1

	After Burn-In Measurements						Post T/S
Serial Number	DC Resistance (Ω)	Δ DCR (%)	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 67 GHz	DC Resistance (Ω)
1	50.55	-0.56	1.04	1.04	1.14	1.13	50.83
2	50.34	-1.07	1.03	1.05	1.16	1.22	50.89
3	51.67	1.53	1.02	1.08	1.18	1.13	50.89
4	50.60	-0.66	1.06	1.08	1.13	1.11	50.94
5	50.88	-0.24	1.06	1.04	1.16	1.10	51.01
6	50.63	-0.44	1.03	1.04	1.13	1.16	50.85
7	50.75	-0.08	1.01	1.06	1.18	1.17	50.79
8	50.70	-0.44	1.05	1.05	1.16	1.11	50.92
9	50.45	-1.23	1.01	1.08	1.18	1.14	51.08
10	49.77	-0.75	1.08	1.01	1.11	1.11	50.15
11	50.63	-0.42	1.03	1.04	1.16	1.17	50.84
12	49.26	-0.82	1.04	1.03	1.14	1.12	49.66
13	50.50	-0.50	1.04	1.05	1.16	1.21	50.75
14	50.72	-0.43	1.03	1.04	1.14	1.16	50.94
15	50.64	-0.49	1.05	1.03	1.14	1.12	50.89
16*	50.69	0.01					50.68
17*	50.11	0.01					50.11
18*	50.80	0.02					50.79
19*	51.08	0.01					51.07
20*	51.09	0.01					51.08

Table 5. Group A Post Burn In Electrical Test Results - Summary

Note: Fifteen devices were subjected to this test due to capacity limitations. These devices show DCR measurements to verify test methods as DC Resistance showed changes in both directions. Devices were remeasured with 4-wire leads directly to PCB line. These measurements were consistent with the resistance changes measured using the PCB and connector loss (original) method.

Further testing (groups B and C) tested the resistance directly to PCB line at risk of damaging it as DCR through the connector method (see Figure 21) showed variation through the connector mounting and re-mounting.

Figure 21. Four-wire resistance measurement of DUTs

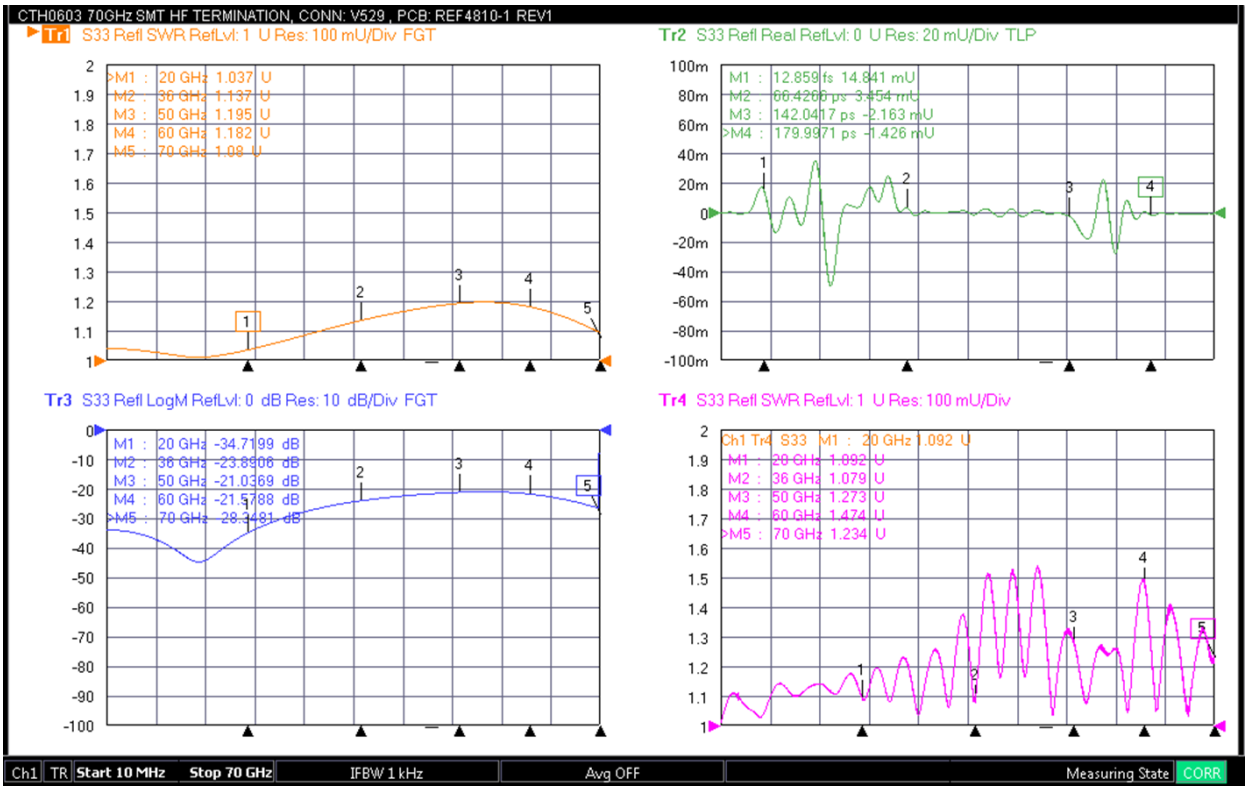


Figure 22. Group A Post Burn In Electrical Test Results – RF performance of a typical sample from the inspection lot: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

Percent Defective Allowable (PDA) Analysis Results

Percentage Defective Allowable (PDA) Analysis was performed on the Group A inspection lot. The defective percentage was calculated to be 0% which is below an acceptable 10%. It was concluded that the inspection lot that was subjected to the test passed the Group A testing and could be moved over to the Group B test stage.

GROUP B INSPECTION (10 samples):

Ten (10) samples from the Group A inspection lot were randomly selected. The 10-sample lot was divided into three subgroups – subgroup 1 (quantity 2), subgroup 2 (quantity 5), and subgroup 3 (quantity 3).

SUBGROUP 1 (2pc sample) TEST RESULTS

Resistance to Temperature Characteristics

Devices were tested in accordance with MIL-STD-202, Method 304. The test was performed according to the following details and exceptions:

- Reference temperature: room ambient temperature.
- Test temperatures:
  - Step 1: room temperature.
  - Step 2: –55°C.
  - Step 3: room temperature.
  - Step 4: +125°C.
- Accuracy of temperature measurement: Devices were maintained within 3˚C of each test temperature for a period of 30 to 45 minutes. Acceptance limits: per the SCD.

The thermal chamber used is shown in Figure 23, the RF performance at three temperature levels presented in Figures 24-26, and the test summary in the Table 6. As shown in the test results below, the inspection lot samples passed the requirements.

Figure 23. Devices under test in the thermal chamber

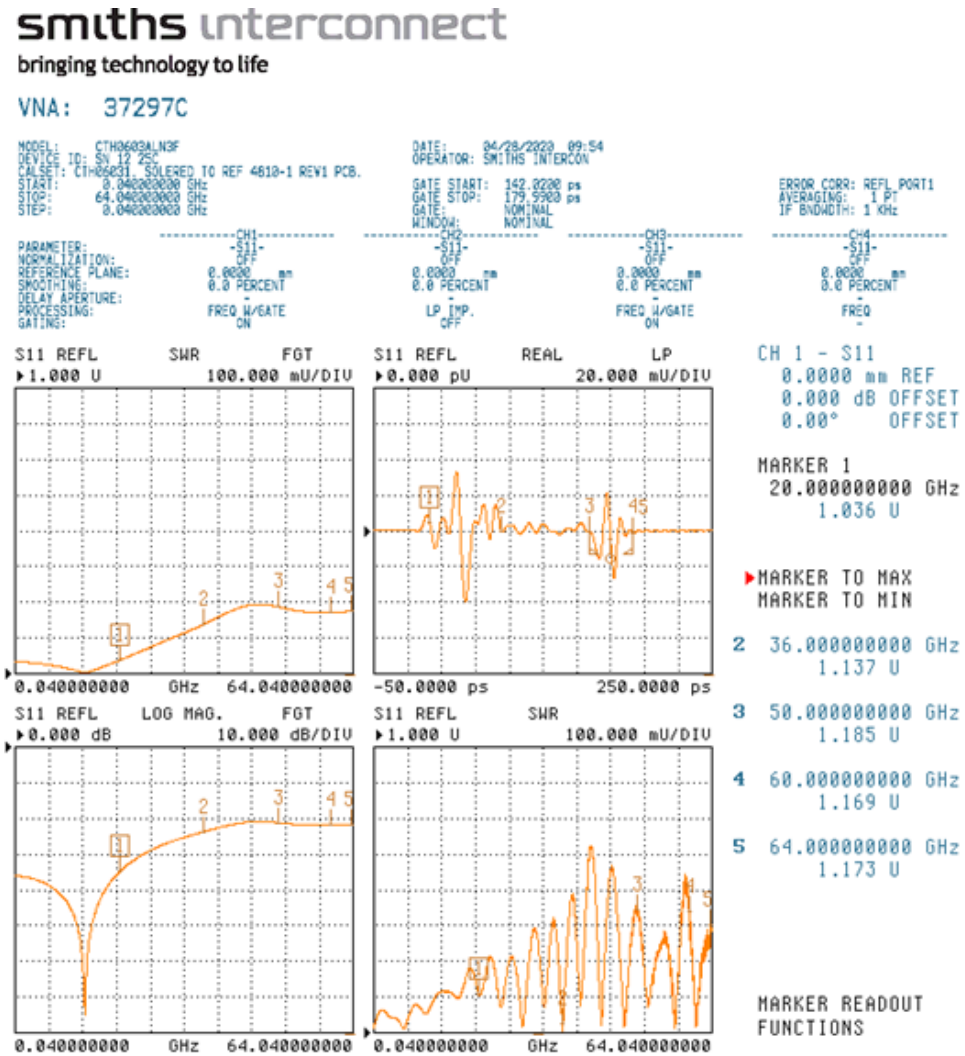


Figure 24. Typical RF performance of the Group B, subgroup 1 sample at Room (+25°C) Temperature: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

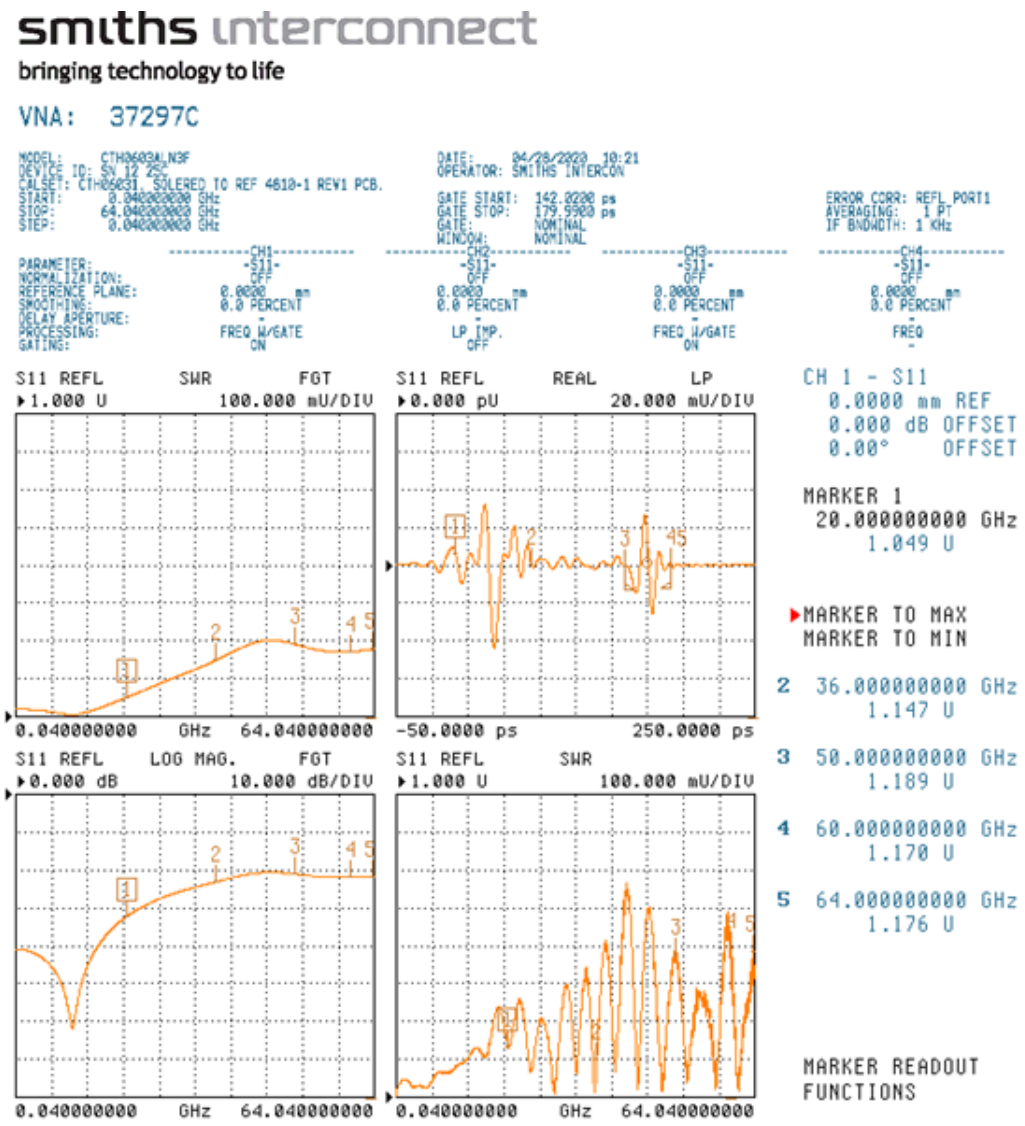


Figure 25. Typical RF performance of the Group B, subgroup 1 sample at Cold (-55°C) Temperature: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

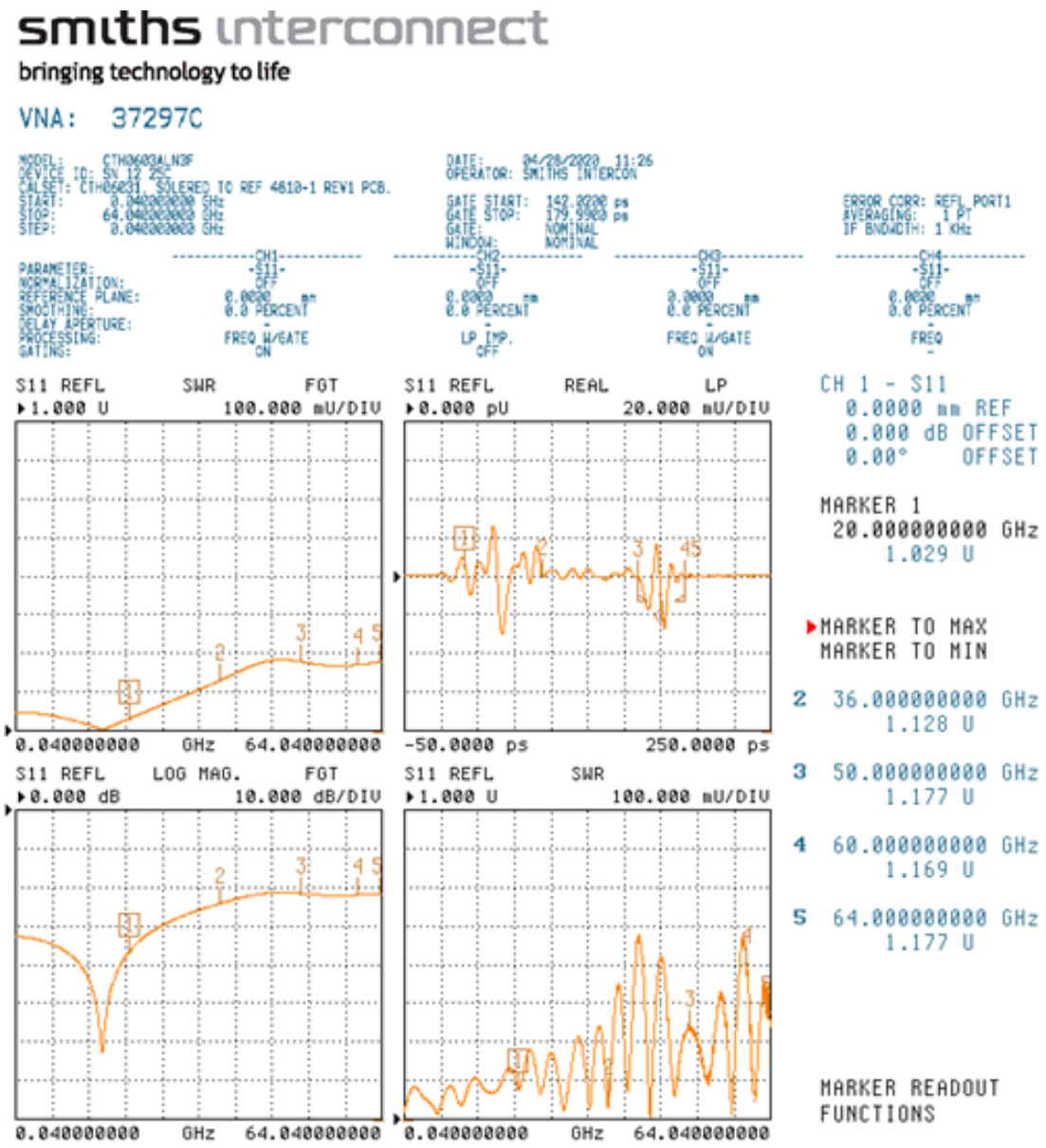


Figure 26. Typical RF performance of the Group B, subgroup 1 sample at Hot (+125°C) Temperature: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

HF Series Terminations per Test Plan TP-9275		smiths interconnect bringing technology to life	
Test Group	B	Part Number	CTH0603ALN3SMTF
Test Sequence	B1-1	Description	70GHz HF Termination, SMT
Test Step	Resistance to Temperature Characteristics	Revision	-
Quantity	2	Test Plan	TP-9275
Date In	4/27/2020	Factory Order	REF 4796
Date Out	4/27/2020	Lot Code	16522
Operator	JA	Results	Pass

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	200	ppm/°C (±)
VSWR Limit	1.50	:1

Note: Gated VSWR reported.

Devices S/N11 & S/N 12 were temperature tested simultaneously using the Thermonics TE-2100E temp forcing system.

	25C	-55C	RTC Cold
Serial Number	DC Resistance (Ω)	DC Resistance (Ω)	Δ DC Resistance (ppm)
11	50.676	51.024	8.58

	25C	+125C	RTC Hot
Serial Number	DC Resistance (Ω)	DC Resistance (Ω)	Δ DC Resistance (ppm)
11	50.693	50.309	-7.58

	25C Return
Serial Number	DC Resistance (Ω)
11	50.659

25C Initial	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 64.04 GHz
12	1.05	1.12	1.04	1.31

-55C	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 64.04 GHz
12	1.04	1.05	1.15	1.18

25C	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 64.04 GHz
12	1.05	1.12	1.04	1.31

125C	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 64.04 GHz
12	1.06	1.03	1.13	1.18

25C Return	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 64.04 GHz
12	1.05	1.04	1.14	1.17

Table 6. Group B, Subgroup 1 Test over Temperature Results - Summary

SUBGROUP 2 (5pc sample) TEST RESULTS

Low Temperature Operation Test Results

DC resistance between the input port and the ground path (Figure 17) was measured and recorded in accordance with MIL-STD-202, Method 303. After the devices were mounted to the heatsink and allowed to stabilize at -55˚C +0˚/-5˚C for one hour (see Figure 27), the full rated DV voltage was applied for a duration of 45 minutes as per MIL-PRF-55342, Par 4.8.5. The DC resistance path was measured before and after the stabilization at 25˚C and recorded in accordance with MIL-STD-202, Method 303. Acceptance limits: per the SCD plus DC resistance Δ ±0.5 % from the previous electrical test. As shown in Table 7, the 5-sample inspection lot passed the requirements.

Figure 27. Test setup for low temperature operation test

HF Series Terminations per Test Plan TP-9270			smiths interconnect bringing technology to life		
Test Group	B	Part Number	CTH0603ALN3SMTF		
Test Sequence	B2-2	Description	70GHz HF Termination, SMT		
Test Step	Low Temperature Operation	Revision	-		
Quantity	5	Test Plan	TP-9275		
Date In	4/15/2020	Factory Order	REF 4796		
Date Out	4/17/2020	Lot Code	16522		
Operator	JA	Results	Pass		
Nominal Resistance Value	50	Ω			
Upper Limit DCR	55	Ω			
Lower Limit DCR	45	Ω			
Delta DCR	0.50	% (±)			
Power Handling	1	W			
	After Low Temp Op		Initial		
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)	Δ DCR ABI - BLTO (%)	ABI Final
6	50.59	0.00	50.59	-0.09	50.63
7	50.71	0.00	50.71	-0.07	50.75
8	50.67	0.01	50.66	-0.07	50.70
9	50.43	0.00	50.43	-0.05	50.45
10	49.73	0.01	49.72	-0.09	49.77

Table 7. Group B, Subgroup 2 Initial Electrical Results - Summary

Peak Power Test Results

The devices were mounted on a suitable heatsink and subjected to peak power with the following characteristics DC pulse characteristics: 10 ms pulse duration and 1% duty cycle (1millisecond period) at ten times (10X) the maximum continuous power of 1 W, as per MIL-DTL-3933, Par 4.7.11.7. Devices were mounted on a suitable heatsink (see Figure 28).

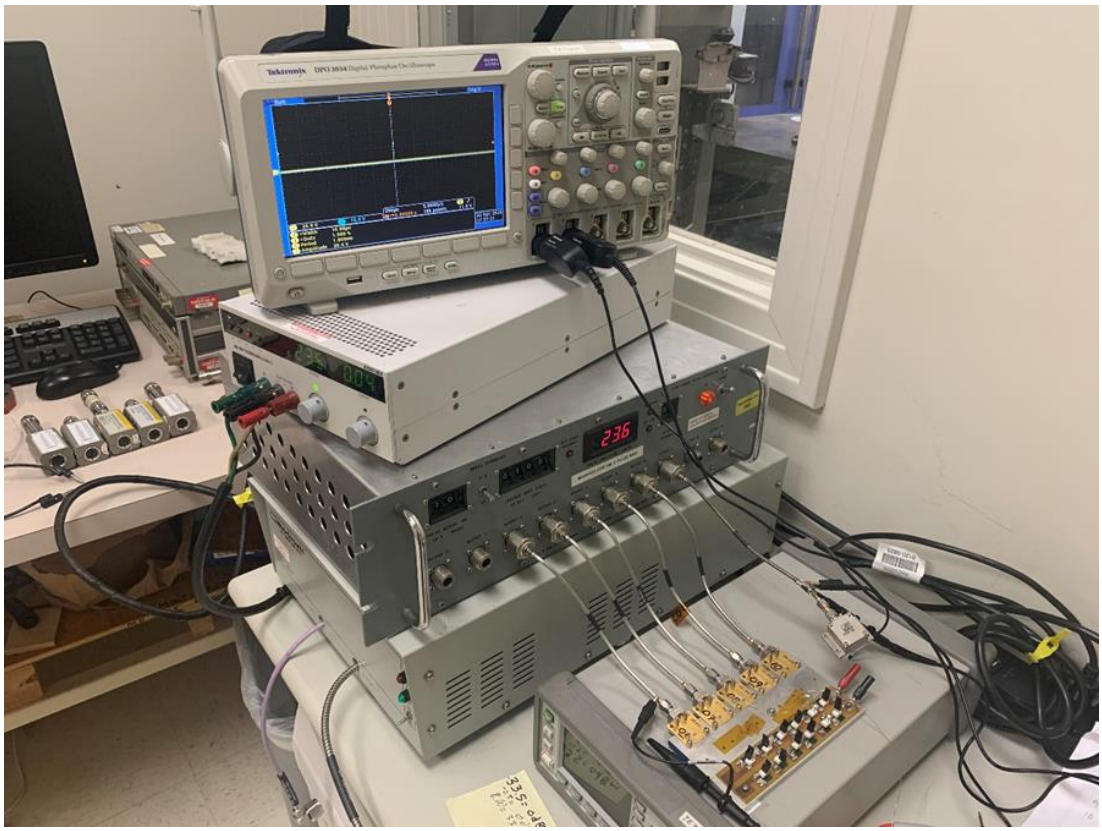


Figure 28. Peak Power Test Setup

DC resistance between the input port and the ground path (Figure 17) was measured and recorded in accordance with MIL-STD-202, Method 303. Acceptance limits as per the SCD plus DC resistance Δ ±0.8 % from the previous electrical test. As shown in Table 8, the 5-sample inspection lot passed the requirements.

HF Series Terminations per Test Plan TP-9270			
Test Group	B	Part Number	CTH0603ALN3SMTF
Test Sequence	B2-4	Description	70GHz HF Termination, SMT
Test Step	Peak Power Test	Revision	-
Quantity	5	Test Plan	TP-9275
Date In	4/17/2020	Factory Order	REF 4796
Date Out	4/20/2020	Lot Code	16522
Operator	JA	Results	Pass

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	0.80	% (±)
Power Handling*	11	W

Note: Due to pulse tester minimum voltage applied was 23.5V or 11.045 W for 1Hr. 20 Mins.

	After Peak Power Test		Initial (ALTO)
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)
6	50.93	0.68	50.59
7	50.74	0.05	50.71
8	50.67	0.00	50.67
9	50.76	0.67	50.43
10	49.73	0.00	49.73

Table 8. Group B, Subgroup 2 Post Peak Power Electrical Test Results - Summary

High Temperature Exposure Test Results

The devices were subjected to 150°C ±5°C for a period of 100 hours ±4 hours per MIL-PRF-55342, Method 4.8.7. DC resistance between the input port and the ground path (Figure 17) was measured and recorded in accordance with MIL-STD-202, Method 303. Acceptance limits were as per the SCD plus DC resistance Δ ±0.5 % from the previous electrical test. As shown in Table 9, the 5-sample inspection lot passed the requirements.

HF Series Terminations per Test Plan TP-9275							
Test Group	B	Part Number	CTH0603ALN3SMTF				
Test Sequence	B2-6	Description	70GHz HF Termination, SMT				Summary Sheet
Test Step	High Temperature Exposure	Revision	-				Test Conditions
Quantity	5	Test Plan	TP-9275				
Date In	4/22/2019	Factory Order	REF 4796				
Date Out	4/29/2020	Lot Code	16522				
Operator	JA	Results	Pass				

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	0.50	% (±)
VSWR Limit	1.50	:1

	After High Temperature Exposure		Initial (APC)	VSWR (AHTE)			
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)	VSWR @ 1GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 67 GHz
6	51.06	0.25	50.93	1.03	1.04	1.13	1.14
7	50.81	0.13	50.74	1.01	1.06	1.17	1.11
8	50.77	0.20	50.67	1.04	1.04	1.15	1.16
9	50.90	0.26	50.76	1.01	1.08	1.17	1.10
10	49.84	0.22	49.73	1.07	1.02	1.11	1.11

Table 9. Group B, Subgroup 2 Post High Temperature Exposure Electrical Test Results - Summary

Final RF Test (RF FIN)

VSWR performance (or Return Loss [RL]) of the DUTs was measured and recorded at low, mid and high frequencies on a Vector Network Analyzer (VNA), in accordance with MIL-STD-39030, Method 4.6.10. S-parameter files are captured for each device. Acceptance limits were as per the SCD. The results are shown in Table 9 and Figure 29.

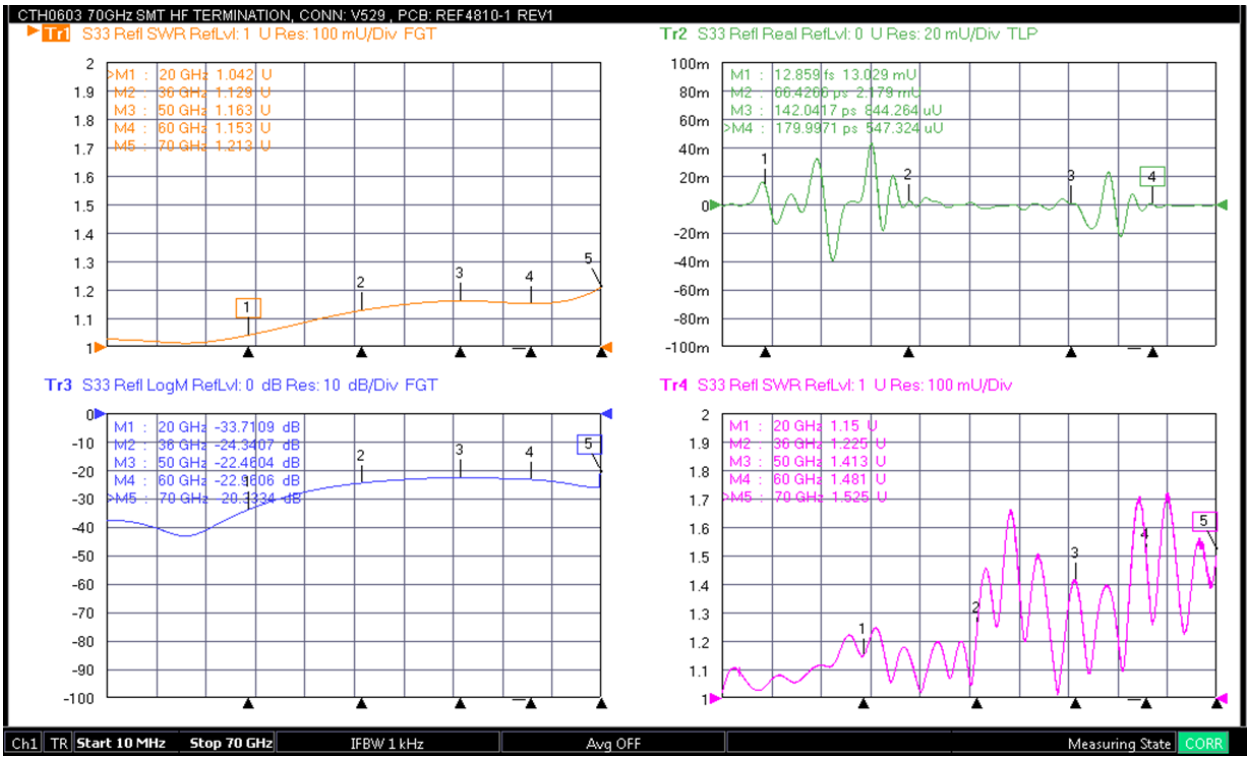


Figure 29. Typical RF performance of the Group B, subgroup 2 sample at Final RF Test: gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

SUBGROUP 3 (3pc sample) TEST RESULTS

Solder Mounting Integrity Test Results:

Devices were soldered to a suitable substrate. A .75-kilogram force was applied to the chip edge for 30 seconds per MIL-PRF-55342, Method 4.8.13.1. The devices were then visually inspected for any evidence of mechanical damage. As indicated in Table 10, the subgroup 3 devices passed the test.

HF Series Terminations per Test Plan TP-9275			smiths interconnect bringing technology to life
Test Group	B	Part Number	CTH0603ALN3SMTF
Test Sequence	B3-2	Description	70GHz HF Termination, SMT
Test Step	Solder Mounting Integrity	Revision	-
Quantity	3	Test Plan	TP-9275
Date In	5/8/2020	Factory Order	REF 4796
Date Out	5/8/2020	Lot Code	16522
Operator	TFM	Results	Pass
Pull Strength	0.75	kg.	
Duration	30	secs.	
Serial Number	Solder Mounting Integrity		
13	Pass		
14	Pass		
15	Pass		

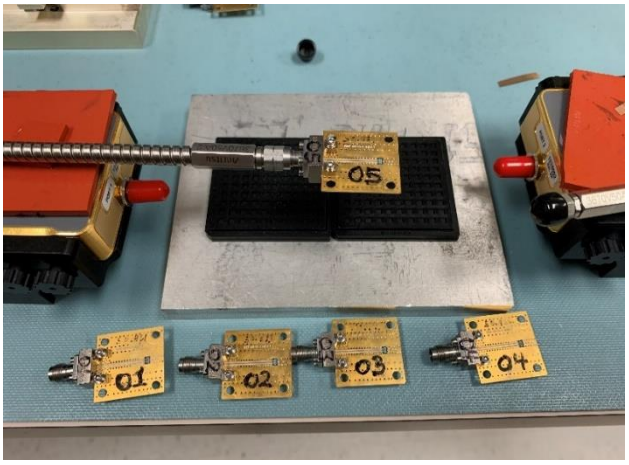
Table 10. Group B, Subgroup 3 Solder Mounting Integrity Test Results - Summary

GROUP C INSPECTION (4 samples):

Group C inspection was conducted on randomly selected samples that have been previously subjected to Group A Inspection.

Life Test (1000 hr Burn-In):

The devices were subjected to the maximum input power specified in the SCD by applying the equivalent DC voltage to properly mounted devices on a suitable heat sink for a total of 1000 +48/-0 hours at 70°C base temp. The power was continuously increased until the maximum power and base temp were achieved. Electrical (DC Resistance) measurements were made and recorded after 250 +48/-0, 500 +48/-0, and 1000 +48/-0 hours. Acceptance limits were as per the SCD plus DC Resistance Δ $\pm$0.5 % from after previous electrical test.



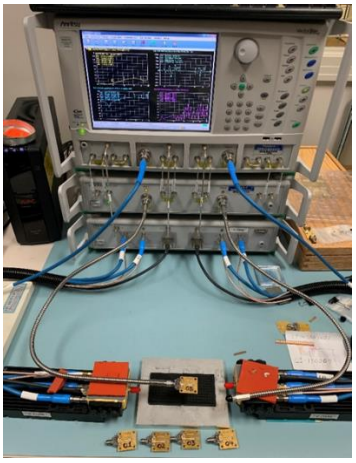


Figure 30. Group C samples

HF Series Terminations per Test Plan TP-9275

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Test Group	C	Part Number	CTH0603ALN3SMTF
Test Sequence	C2	Description	70GHz HF Termination, SMT
Test Step	Life Test	Revision	-
Quantity	5	Test Plan	TP-9275
Date In	3/30/2020	Factory Order	REF 4796
Date Out	5/11/2020	Lot Code	16522
Operator	JA	Results	Pass

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	0.50	% (±)
Power Handling	1	W

4/9/2020	After 250 (234 actual) Hours		Initial
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)
1	50.50	-0.01	50.50
2	50.28	-0.04	50.30
3	51.61	-0.01	51.62
4	50.54	0.00	50.54
5	50.81	0.00	50.82

4/21/2019	After 500 (524 actual) Hours		234 Hours
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)
1	50.47	-0.04	50.50
2	50.27	-0.02	50.28
3	51.59	-0.04	51.61
4	50.54	-0.01	50.54
5	50.80	-0.03	50.81

5/11/2020	After 1000 Hours		524 Hours
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)
1	50.44	-0.07	50.47
2	50.21	-0.10	50.27
3	51.55	-0.07	51.59
4	50.51	-0.07	50.54
5	50.79	-0.03	50.80

Table 11. Group C After 1000 hour Life Test Electrical Results - Summary

VSWR performance (or Return Loss) of the DUTs was measured and recorded at low, mid and high frequencies on a Vector Network Analyzer (VNA), in accordance with MIL-STD-39030, Method 4.6.10. S-parameter files are captured for each device. Acceptance limits as per the SCD. The results are presented in Table 12 and Figure 31; as observed, the group C samples passed the acceptance limits.

HF Series Terminations per Test Plan TP-9275

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Test Group	C	Part Number	CTH0603ALN3SMTF
Test Sequence	C3	Description	70GHz HF Termination, SMT
Test Step	Post Life Electrical (DC & RF) Inspection	Revision	-
Quantity	5	Test Plan	TP-9275
Date In	5/11/2020	Factory Order	REF 4796
Date Out	5/11/2020	Lot Code	16522
Operator	JA	Results	Pass

Nominal Resistance Value	50	Ω
Upper Limit DCR	55	Ω
Lower Limit DCR	45	Ω
Delta DCR	0.50	% (±)
VSWR Limit	1.50	:1

	After 1000 hr Life Test		Life Test 0Hrs	VSWR (ALT)			
Serial Number	DC Resistance (Ω)	Δ DC Resistance (%)	DC Resistance (Ω)	VSWR @ 1 GHz	VSWR @ 20 GHz	VSWR @ 36 GHz	VSWR @ 67 GHz
1	50.44	-0.12	50.50	1.03	1.05	1.14	1.15
2	50.21	-0.17	50.30	1.02	1.07	1.18	1.23
3	51.55	-0.12	51.62	1.01	1.09	1.18	1.17
4	50.51	-0.08	50.54	1.04	1.07	1.14	1.13
5	50.79	-0.06	50.82	1.04	1.05	1.15	1.13

Table 12. Post Life Electrical Results - Summary

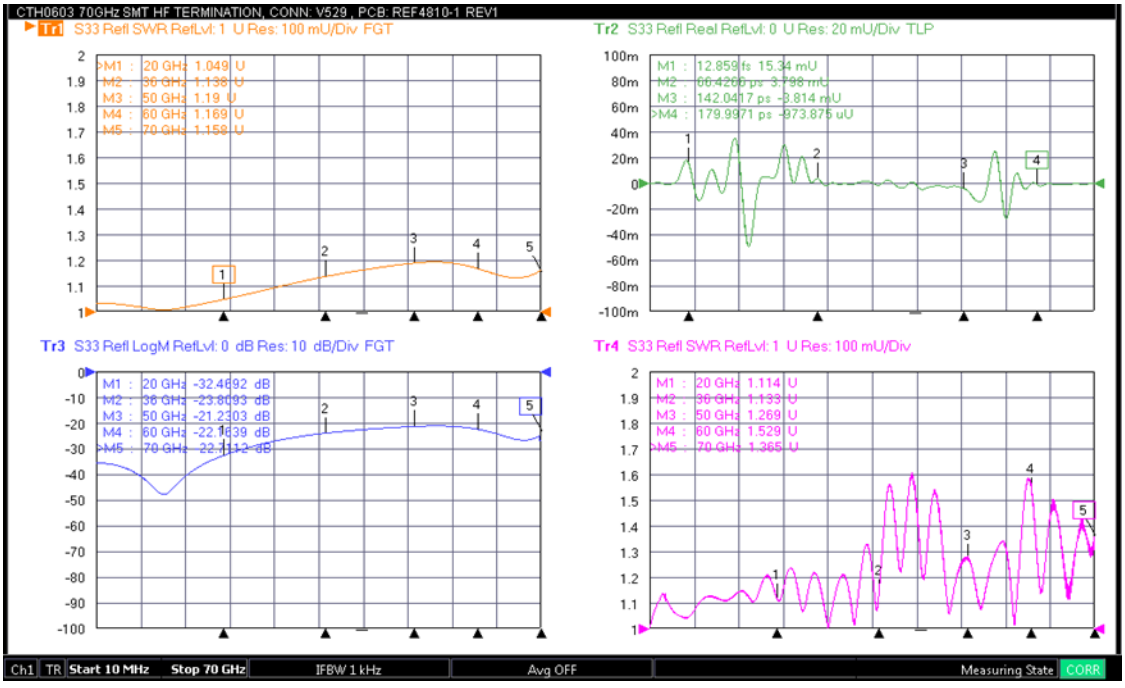

Figure 31. Typical RF performance of the Group C sample after the life test (1000 hr): gated VSWR (top left), gated return loss (bottom left), time domain (top right), ungated VSWR (bottom right)

10. Qualification Test – Summary and Conclusion

The high frequency surface mount RF termination CTH0603ALN1SMTF operating in the frequency band DC–67 GHz has been electrically and thermally tested; the test results presented in this test report are evidence of the performance that meets the required specifications.

A rigorous qualification testing as per TP-9275 has also been performed on a 20-piece inspection lot of the CTH0603ALN1SMTF design. The test consisted of Group A, Group B, and Group C testing; the devices were subjected to thermal shock, burn in test, RF test over temperature, low temperature operation test, peak power test, high temperature exposure test, solder mount integrity test, and life test. The results of these qualification tests have been presented in this report. As shown, the inspection lot passed all the specifications as required by the TP-9275 and corresponding SCD. It has therefore been determined that the product **CTH0603ALN1SMTF is qualified to be released into a full production**.

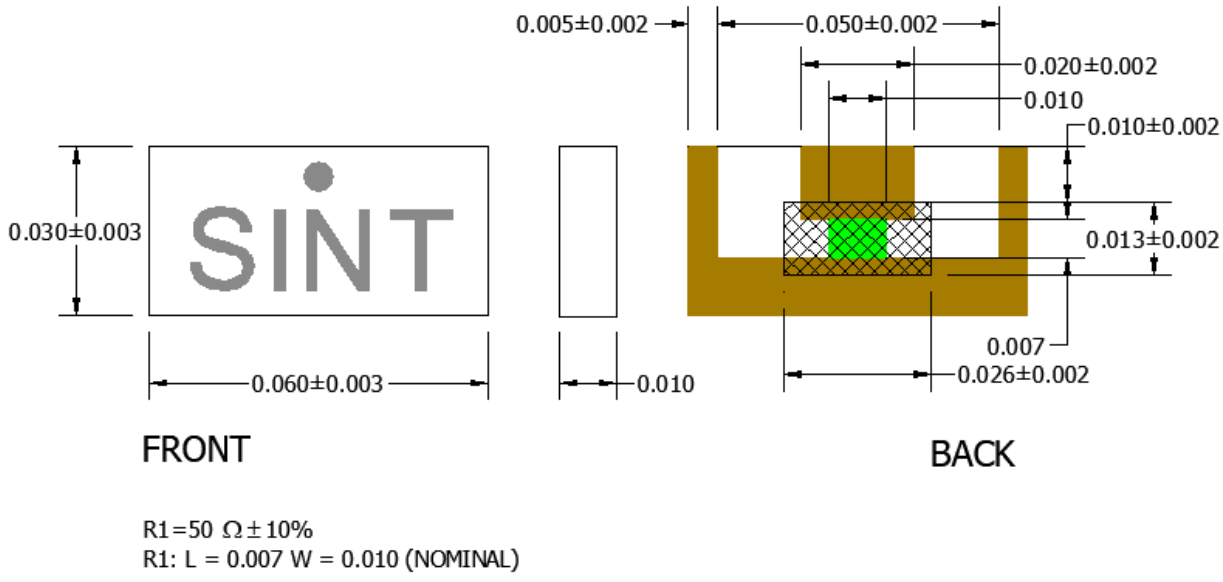

Figure 32. Mechanical layout of the high frequency SMT RF termination CTH0603ALN1SMTF