smiths interconnect

Electrical and Thermal Test Report

High Frequency Chip Equalizers Electrical and Thermal Test Report

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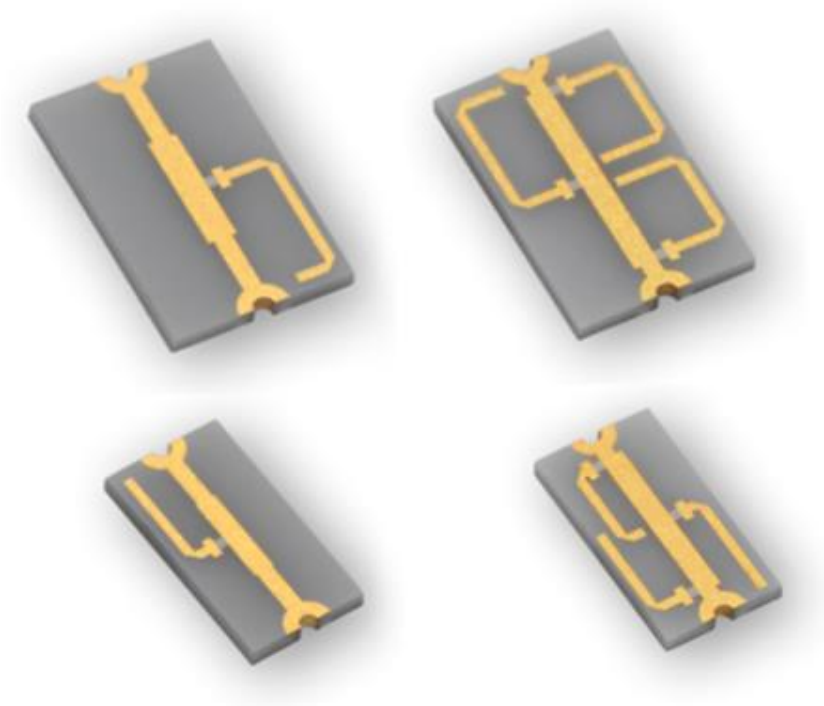
Revision -



1. Scope

The purpose of this test report is to present the electrical and thermal performance of high frequency equalizers developed under the project DD-217490. The report includes the test data collected during the tests performed on these products. Both the pre-test simulation analysis as well as the tests on real prototypes will be displayed and analyzed. Finally, the test procedure is included with the test equipment used and best testing practices implemented.

Electrical performance has been evaluated through the simulation analysis and a real-life test of the DUTs in a test fixture on the vector network analyzer. Thermal performance has also verified through the real-life test. This product, although it contains resistive elements, should be considered a distributive element as the full RF or DC power does not run through the resistive elements. Therefore, a qualification has been performed through a set of tests that make sense for this type of the product.

The test samples passed all the qualification test requirements. The test results that will be presented in this test report are an evidence of a successful test and viability of this product to be released into customers' applications.

2. Specifications

To verify the design recipe developed for a rapid custom modeling and prototyping of this product line as per specific customer order, four different designs have been modeled, manufactured and tested. The frequency bands selected for the design verification were Band 1 (17-22 GHz) and Band 3 (27-32 GHz). The specifications for these designs (CEHF1170P220SMTF, CEHF3170P220SMTF, CEHF1270P320SMTF, and CEHF3270P320SMTF) are shown in Tables 1 through 4, respectively. The size of these components are identical to the sizes of K2TVA products covering the same bands:

- Band 1: 0.140"×0.090"×0.010"
- Band 3: 0.120"×0.065"×0.010".

These products were made using a thin-film based processes on an Alumina ceramic substrate. Detailed specifications for these four products are shown in Tables and Figures below.

Table 1 – Compliance Matrix Electrical Performance (Design 1: CEHF1170P220SMTF)

ITEM	PARAMETER	REQUIREMENT	LIMITS	UNITS	COMPLIANCE (BY TEST)
1	Characteristic Impedance	50	-	Ω	Yes
2	Operating Frequency	17.0 – 21.0	-	GHz	Yes
3	VSWR	1.50:1	maximum	-	Yes
4	Insertion Loss	0.50	maximum	dB	Yes
5	Slope	1.50	maximum	dB	Yes
6	Slope Linearity	±0.50 dB or Better	minimum	mW	Yes
7	Input Power	200	minimum	mW	Yes

8	Operating Temperature	-55 to +150	-	°C	Yes
9	Non-Operating temperature	-65 to +150	-	°C	Yes

Table 2 – Compliance Matrix Electrical Performance (Design 1: CEHF3170P220SMTF)

ITEM	PARAMETER	REQUIREMENT	LIMITS	UNITS	COMPLIANCE (BY TEST)
1	Characteristic Impedance	50	-	Ω	Yes
2	Operating Frequency	17.0 – 21.0	-	GHz	Yes
3	VSWR	1.50:1	maximum	-	Yes
4	Insertion Loss	0.75	maximum	dB	Yes
5	Slope	3.75	maximum	dB	Yes
6	Slope Linearity	±0.50 dB or Better	minimum	mW	Yes
7	Input Power	200	minimum	mW	Yes
8	Operating Temperature	-55 to +150	-	°C	Yes
9	Non-Operating temperature	-65 to +150	-	°C	Yes

Table 3 – Compliance Matrix Electrical Performance (Design 1: CEHF1270P320SMTF)

ITEM	PARAMETER	REQUIREMENT	LIMITS	UNITS	COMPLIANCE (BY TEST)
1	Characteristic Impedance	50	-	Ω	Yes
2	Operating Frequency	17.0 – 21.0	-	GHz	Yes
3	VSWR	1.50:1	maximum	-	Yes
4	Insertion Loss	0.75	maximum	dB	Yes
5	Slope	1.75	maximum	dB	Yes
6	Slope Linearity	±0.50 dB or Better	minimum	mW	Yes
7	Input Power	200	minimum	mW	Yes
8	Operating Temperature	-55 to +150	-	°C	Yes
9	Non-Operating temperature	-65 to +150	-	°C	Yes

Table 4 – Compliance Matrix Electrical Performance (Design 1: CEHF3270P320SMTF)

ITEM	PARAMETER	REQUIREMENT	LIMITS	UNITS	COMPLIANCE (BY TEST)
1	Characteristic Impedance	50	-	Ω	Yes
2	Operating Frequency	26.0 – 31.0	-	GHz	Yes
3	VSWR	1.50:1	maximum	-	Yes
4	Insertion Loss	0.75	maximum	dB	Yes
5	Slope	3.25	maximum	dB	Yes
6	Slope Linearity	±0.50 dB or Better	minimum	mW	Yes
7	Input Power	200	minimum	mW	Yes
8	Operating Temperature	-55 to +150	-	°C	Yes
9	Non-Operating temperature	-65 to +150	-	°C	Yes

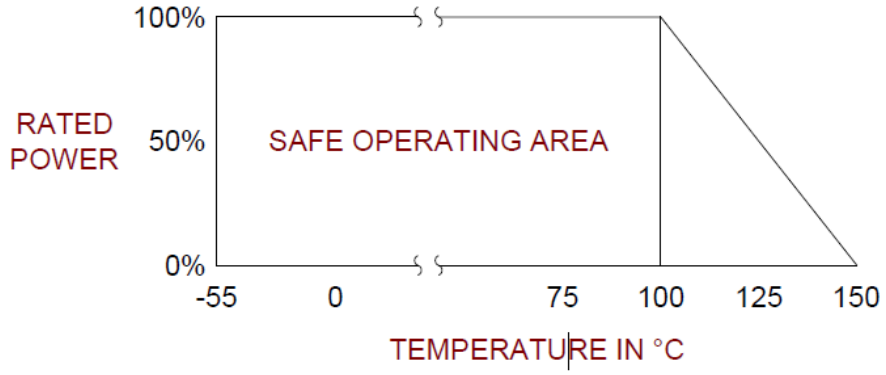


Figure 1 - Power Derating at Temperature

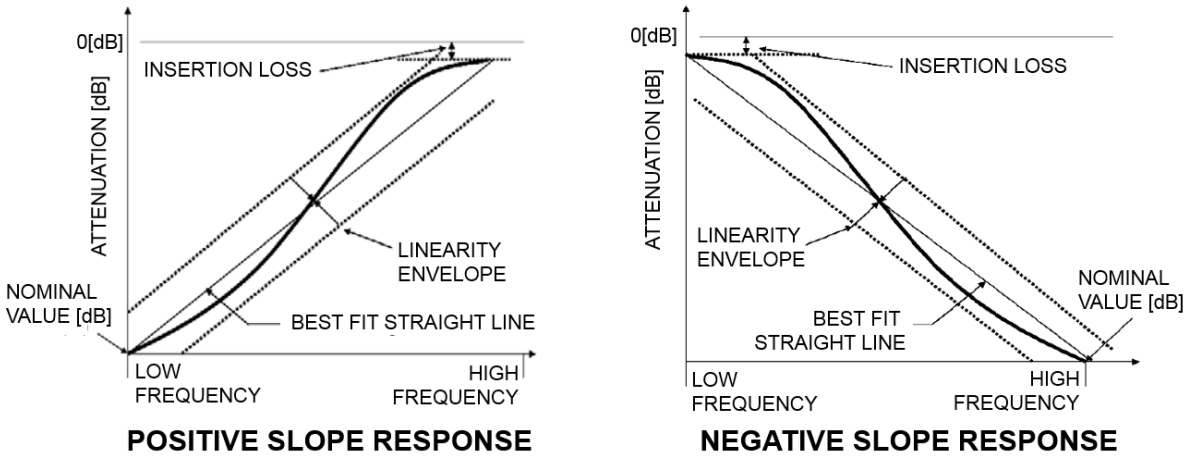
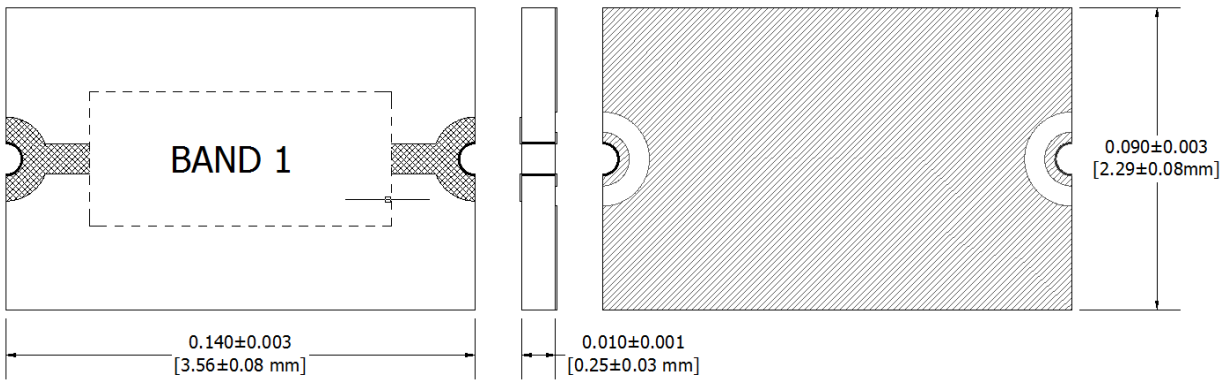


Figure 2. Equalizer - Description of Electrical Parameters



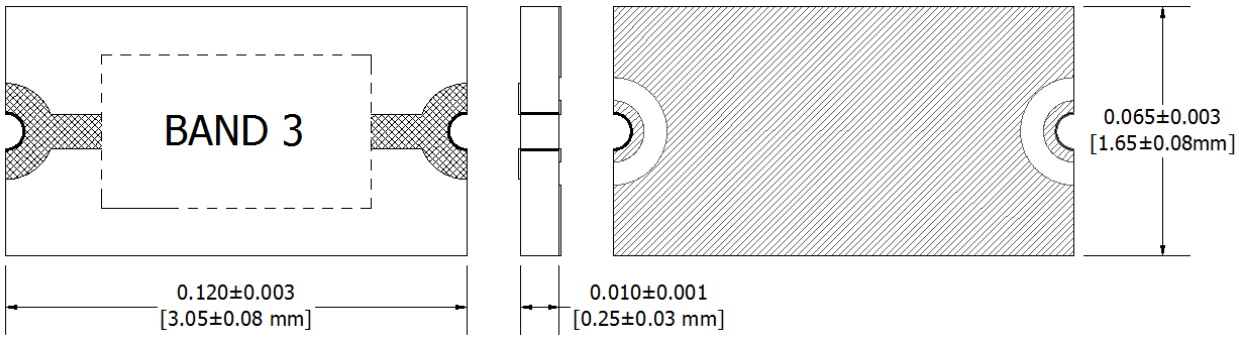
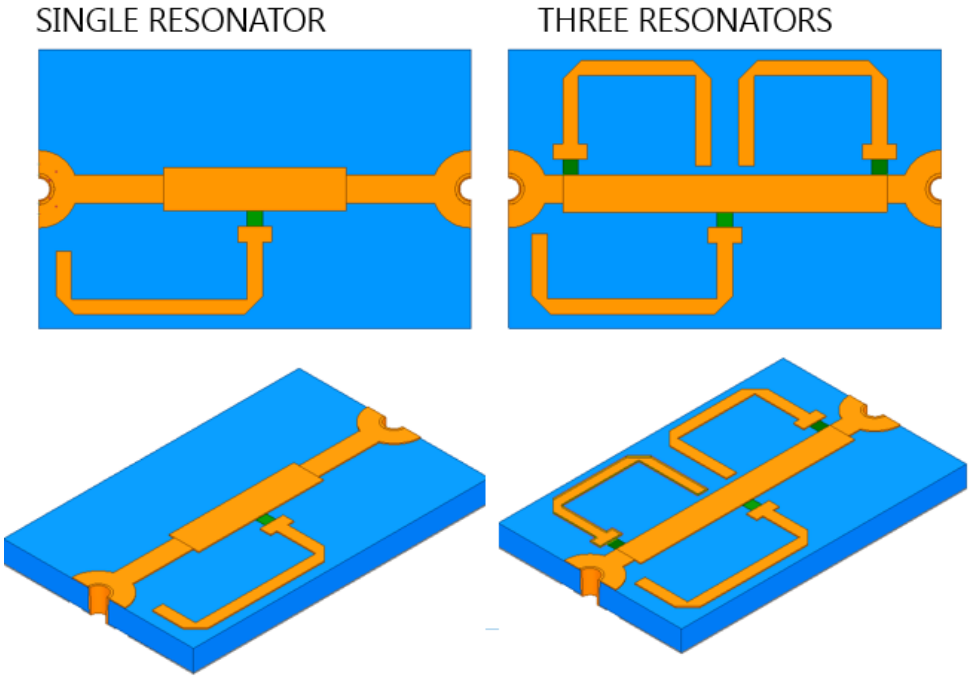


Figure 3. Band 1 and Band 3 Equalizers - Mechanical Footprint

3. Design Verification

To verify the proposed design recipe, four designs have been modeled – two slopes (1 dB and 3 dB) in two frequency bands – Band 1 (17 – 22 GHz) and Band 3 (27 – 32 GHz). All the part numbers have been simulated and tuned in multiple 3D electromagnetic simulator.

- Band 1 (17 – 22 GHz), single resonating element (Part no: CEHF1170P220SMTF)
- Band 1 (17 – 22 GHz), three resonating elements (Part no. CEHF3170P220SMTF)
- Band 3 (27 – 33 GHz), single resonating element (Part no. CEHF1270P320SMTF)
- Band 3 (27 – 33 GHz), three resonating elements (Part no. CEHF3270P320SMTF)



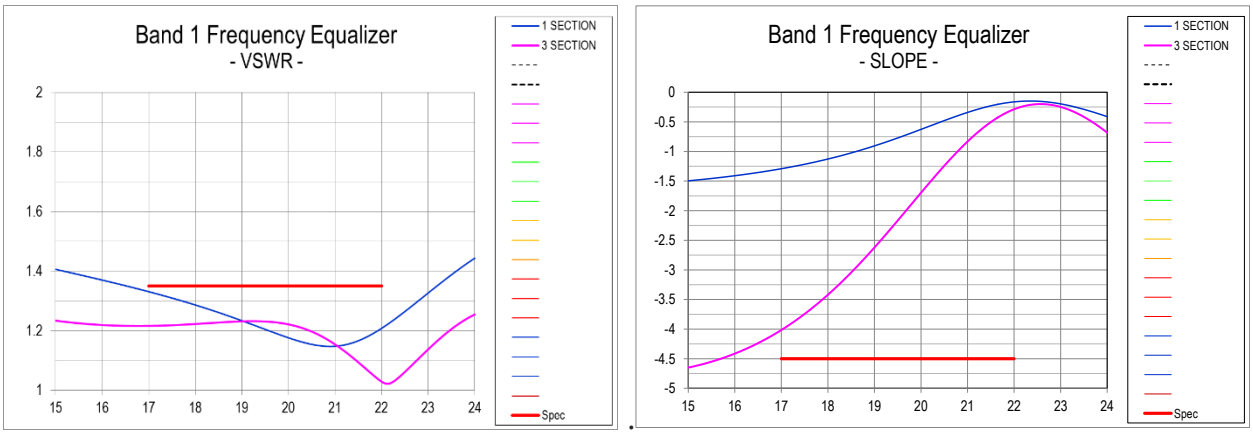
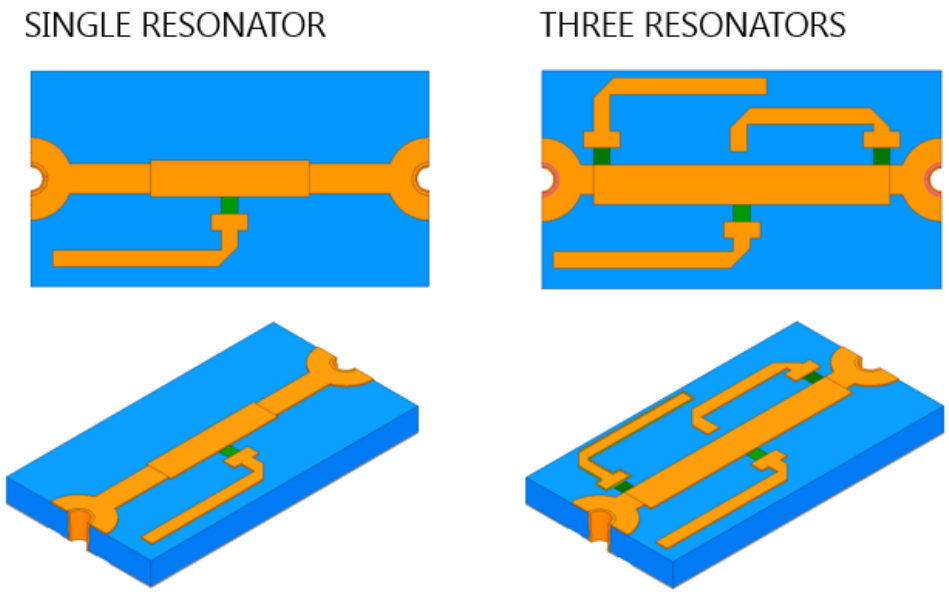


Figure 4. Band 1 Equalizers (one section, three sections): Models and Simulated Electrical Performances



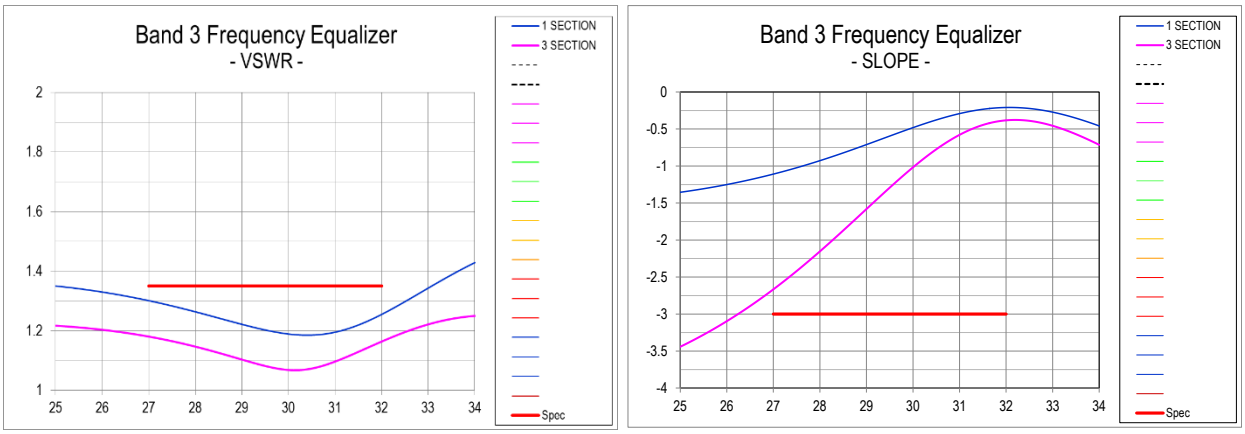
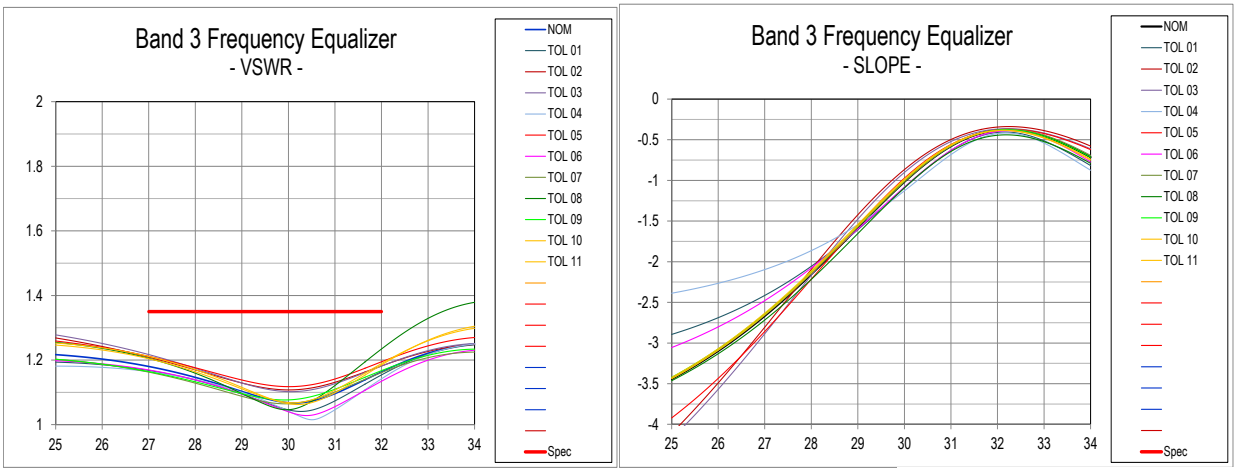


Figure 5. Band 3 Equalizers (one section, three sections): Models and Simulated Electrical Performances

After the designs have been optimized for a nominal performance, the tolerance analysis has been conducted that considered substrate thickness and dielectric constant variations, transmission line dimensional tolerances, and variations in the bulk resistivity and shape of the resistors. For tolerance analysis, Band 3 model with three sections has been chosen as the most critical (smaller size, most complex design).

Figure 10 shows the tolerance analysis results. It can be concluded that the selected model approach results in a very robust design that is not sensitive to the standard manufacturing tolerances.



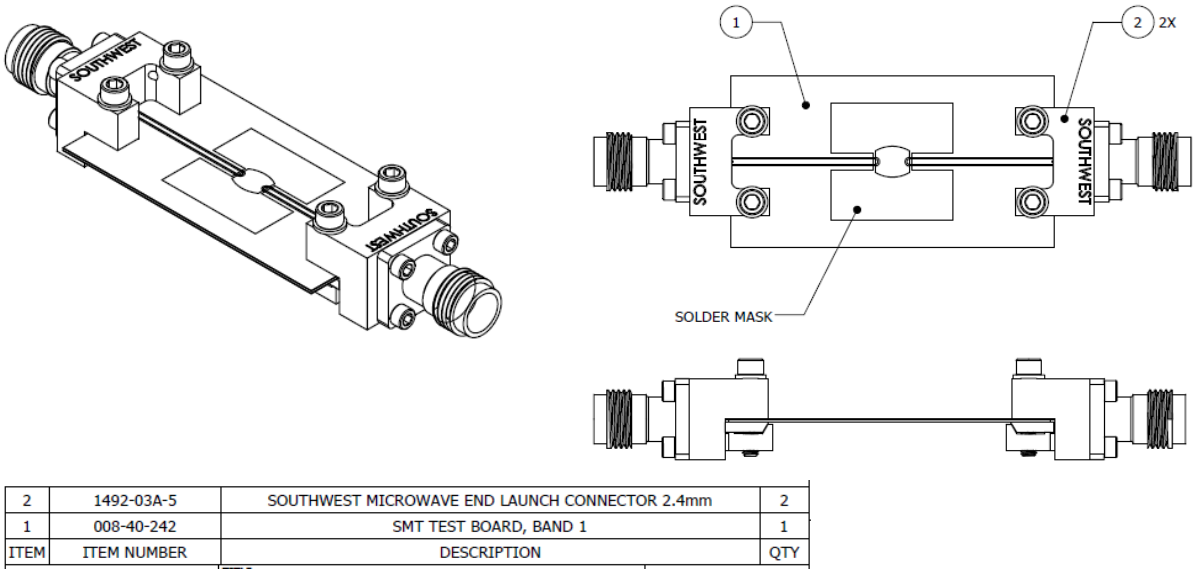
LEGEND:

TOL 01:	resistor value +30%
TOL 02:	resistor value -30%
TOL 03:	resistor width 5 mil + 2 mil
TOL 04:	resistor width 5 mil – 2 mil
TOL 05:	resistor gap (length) 5 mil + 1 mil
TOL 06:	resistor gap (length) 5 mil – 1 mil
TOL 07:	laser drill diameter 10 mil + 1 mil
TOL 08:	laser drill diameter 10 mil – 1 mil
TOL 09:	chip movement 2 mil lateral
TOL 10:	chip movement 2 mil axial
TOL 11:	chip movement 2 mil lateral and axial

Figure 6. Tolerance Analysis Performed on Band 3 Equalizer with Three Sections.

4. Test Fixture Choice

The test fixture that was chosen to test this product was standardized to cover both this product line and the K2TVA surface mount product line in the same two bands (Band 1 and Band 3). The fixture consists of a test board made with Rogers 4350 and two Southwest field replaceable female end launch connectors (1492-03A-5), see Figure 11.



ITEM	ITEM NUMBER	DESCRIPTION	QTY
2	1492-03A-5	SOUTHWEST MICROWAVE END LAUNCH CONNECTOR 2.4mm	2
1	008-40-242	SMT TEST BOARD, BAND 1	1

Figure 7. Test Fixture used to test Developed Prototypes.

The 2.4 mm jack (female) end launch connector used for the tests at frequencies DC – 42.5 GHz is shown in Figure 12. It is important to mention that the selection of the connector pin (see dimensions ϕA) on the connector (1.85mm or 2.4 mm) affects the connector launch performance and thus must be chosen as directed.

DWG No.: 91Y60921

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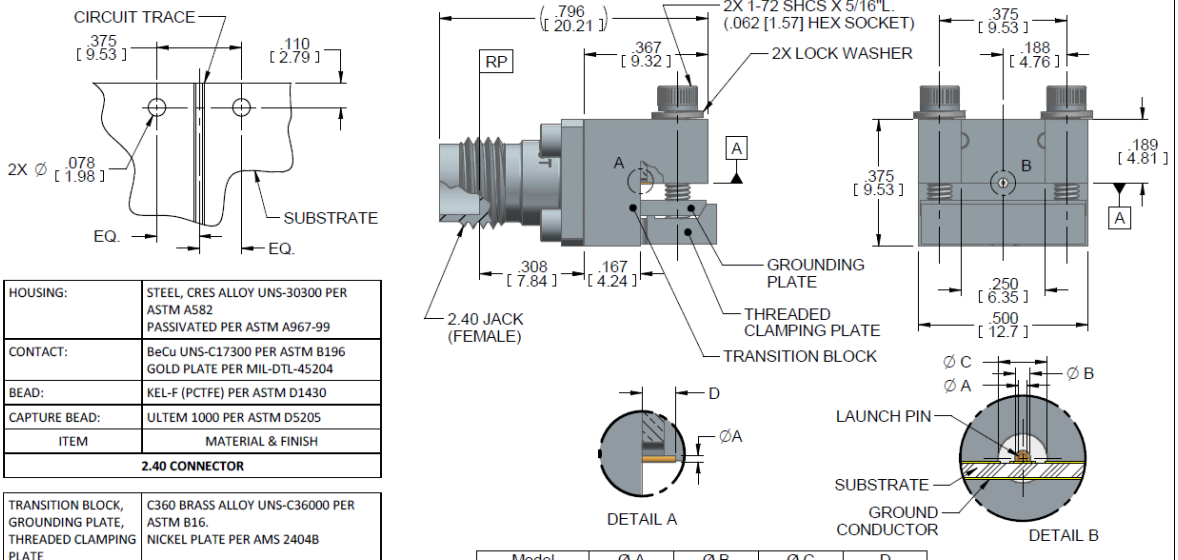

HOUSING:	STEEL, CRES ALLOY UNS-30300 PER ASTM A582 PASSIVATED PER ASTM A967-99
CONTACT:	BeCu UNS-C17300 PER ASTM B196 GOLD PLATE PER MIL-DTL-45204
BEAD:	KEL-F (PCTFE) PER ASTM D1430
CAPTURE BEAD:	ULTEM 1000 PER ASTM D5205
ITEM	MATERIAL & FINISH
2.40 CONNECTOR	

TRANSITION BLOCK, GROUNDING PLATE, THREADED CLAMPING PLATE	C360 BRASS ALLOY UNS-C36000 PER ASTM B16. NICKEL PLATE PER AMS 2404B
LAUNCH PIN:	BeCu UNS-C17300 PER ASTM B196 GOLD PLATE PER MIL-DTL-45204
TRANSITION BLOCK DIELECTRIC:	VIRGIN PTFE FLUOROCARBON PER ASTM D1710, TYPE 1 GRADE 1, CLASS B
ITEM	MATERIAL & FINISH
TRANSITION BLOCK	

1. ALL DIMENSIONS ARE IN INCHES. ALL ANGLES ARE IN DEGREES. DIMENSIONS SHOWN IN BRACKETS [XXX] ARE IN MILLIMETERS.

NOTES: UNLESS OTHERWISE SPECIFIED.

Model	Ø A	Ø B	Ø C	D
1492-02A-5	.010	.020	.0635	.050
1492-01A-5	.007	.015	.0480	.030
1492-03A-5	.007	.012	.0390	.030
1492-04A-5	.005	.009	.0290	.030

REV	RELEASE	APRVD.	DATE:
A		PLC	10/1/12

SOUTHWEST MICROWAVE

Southwest Microwave, Inc.
9055 South McKemy Street
Tempe, Arizona 85284-2946
Telephone (480) 783-0201
Fax (480) 783-0360

TITLE: 2.40mm JACK (FEMALE) END LAUNCH CONNECTOR

DRN BY:	DATE:	DWG. NO.	REV.
EAG	09/28/12	91Y60921	A

SHEET: 1 OF 1

Figure 8. Southwest Microwave 2.4 mm connector used in tests at frequencies DC-42.5 GHz (drawing)

5. Mounting Instructions

First step in properly mounting the chip equalizer for testing is to carefully inspect all the components of the test fixture to be assembled. Special attention should be given to the test board edges (Figure 13a). Common PCB manufacturing often leave rough edges that can cause fixture assembly issues. The edges of the test board can usually be cleaned up using fine grit sand paper. (Figure 13b).

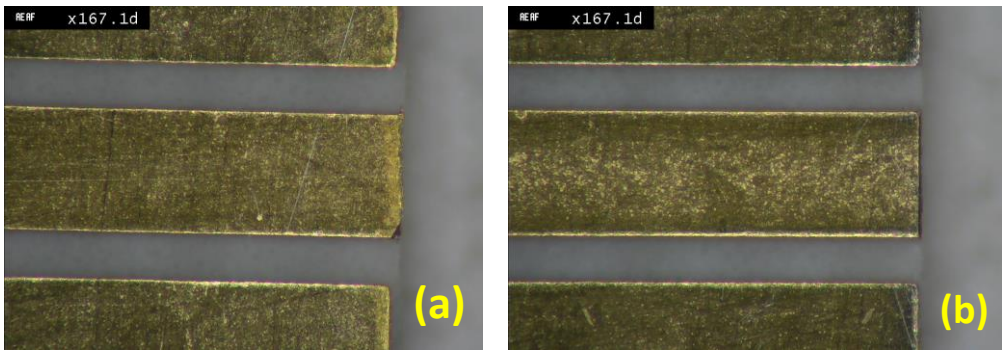

Figure 9. Test board transmission line:
(a) rough edge (before cleaning), (b) smooth edge (after cleaning)

The equalizer should also be inspected to insure the edges are cleanly cut and have no jagged edges prior to being installed on the test board. To avoid any potential electrical failures, the chip equalizer needs to be properly positioned (centered) and soldered in place. Introduction of the solder mask around the footprint area where the equalizer is to be soldered helps this positional alignment. The chip equalizer is soldered onto the test board using Sn96 solder. Care should be taken to insure there is no solder run-out into the area where the DUT is to be mounted.

The final step in the fixture assembly is to mount the connector to the test board. Things to look for at this step is to center the connector pin on the transmission line and to insure the connector is flush with the edge of the test board to avoid undesired air gaps (Figure 14). Use of a microscope is essential to insuring that the connector is mounted properly.

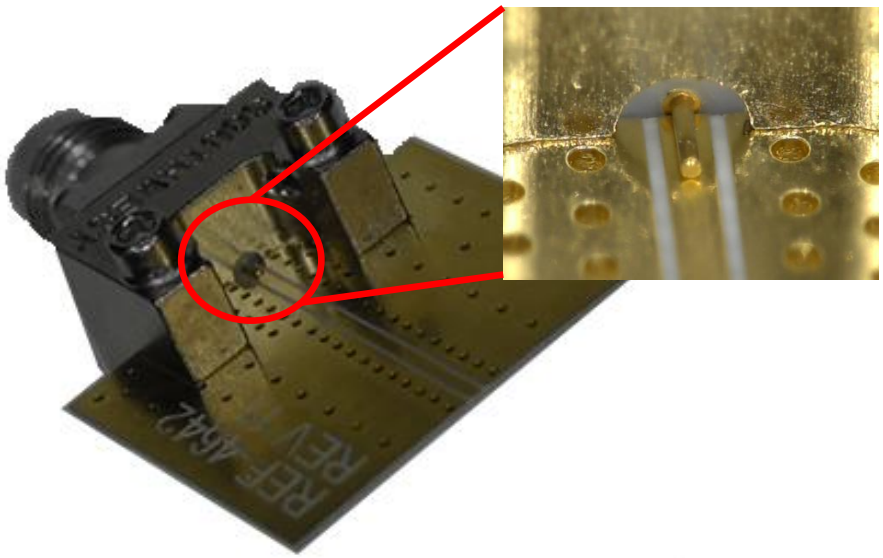

Figure 10. Connector pin alignment on the test board

The mounting instructions are shown on the block diagram (Figure 15). The fully assembled test fixture (Figure 13) consists of the small grounded carrier (3) soldered to the back side of the test board (2) with the RF termination (4) installed using proper mounting practices described above. The Southwest microwave connector (1) is seen on the right side of the fixture.

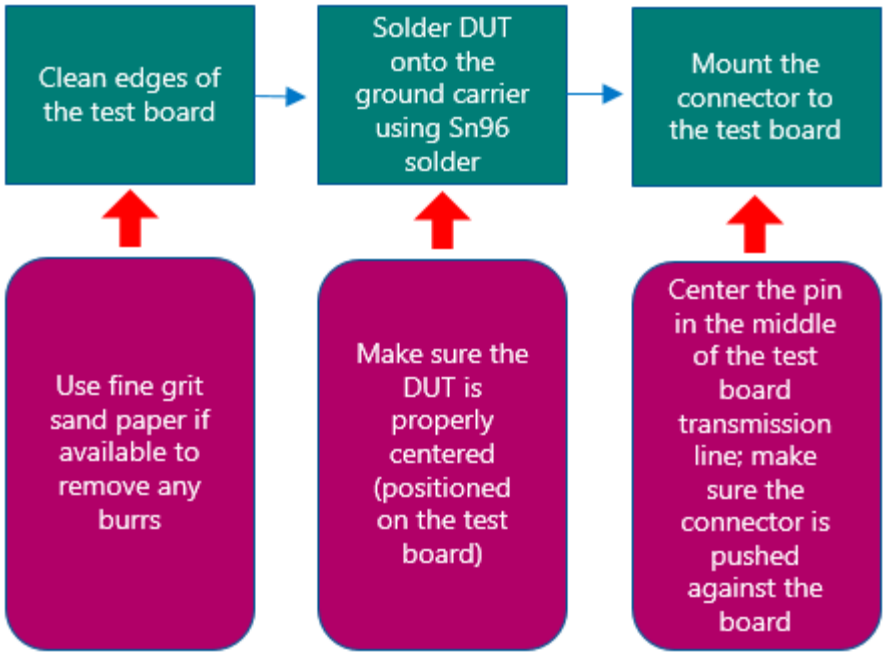

Figure 11. The Mounting instructions – Flow Chart

6. RF Test Results

Five samples of each of the four designs have been successfully installed on the chosen test board and tested over a broad frequency range (DC–40 GHz). The through line (test fixture) loss has also been tested and subtracted from the loss of the DUTs. Typical performance for each dof the four designs is shown in Figures 16-19. The prototypes exhibit a very repetitive performance under for the entire frequency band of interest.

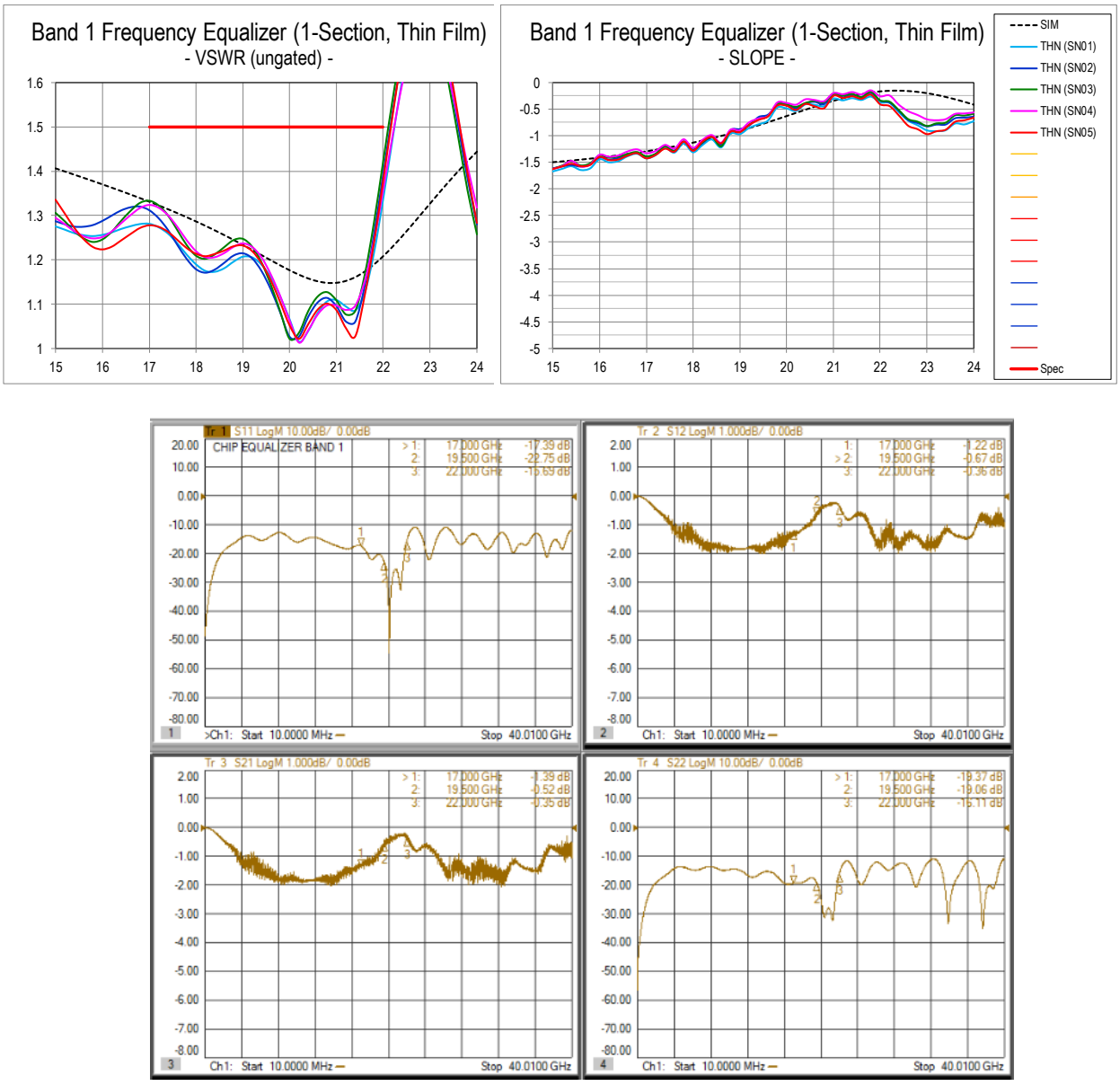

Figure 12. Typical RF performance of CEHF1170P220SMTF: VSWR gated (top left), VSWR ungated (bottom right)

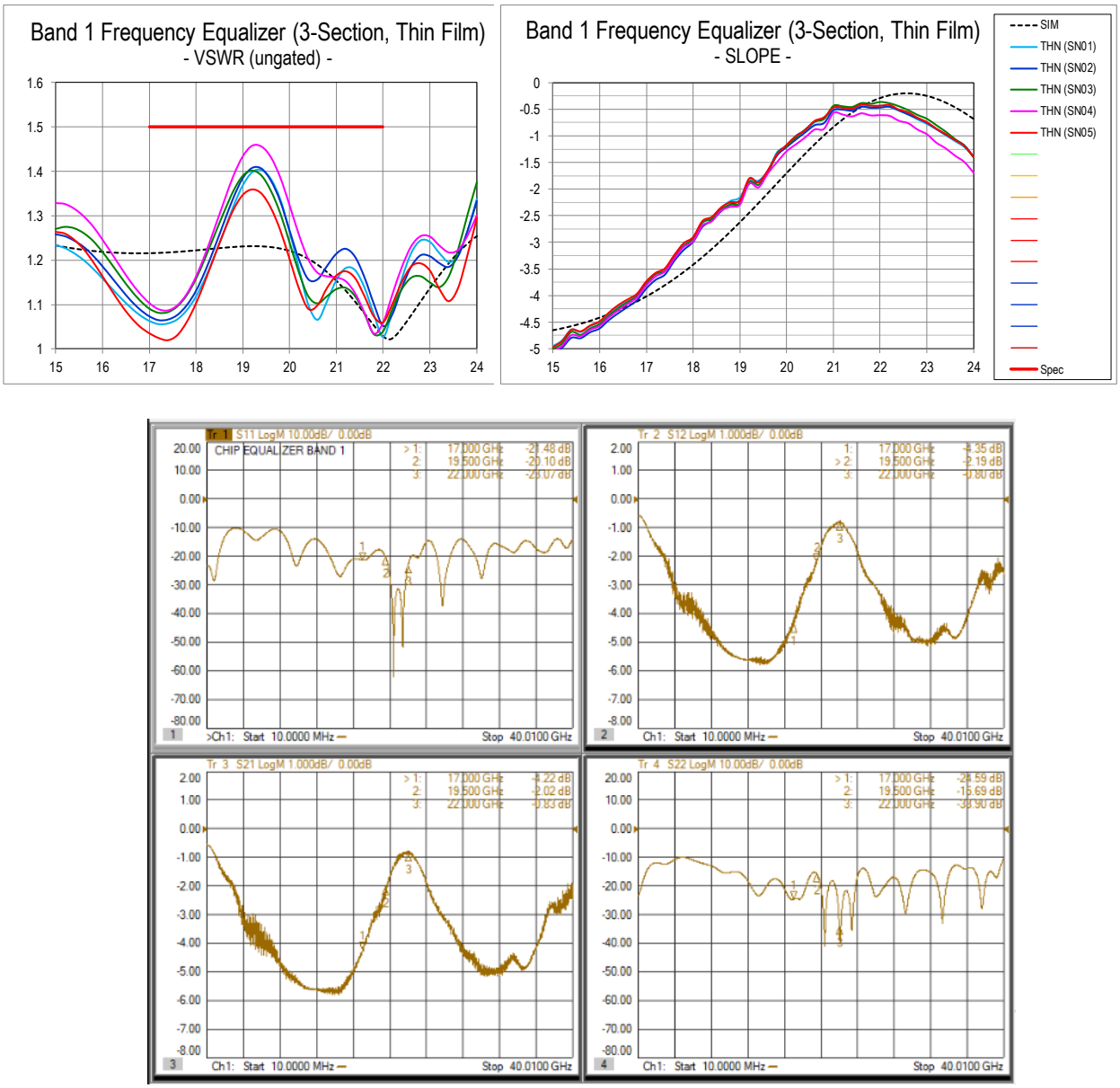

Figure 13. Typical RF performance of CEHF3170P220SMTF: VSWR gated (top left), VSWR ungated (bottom right)

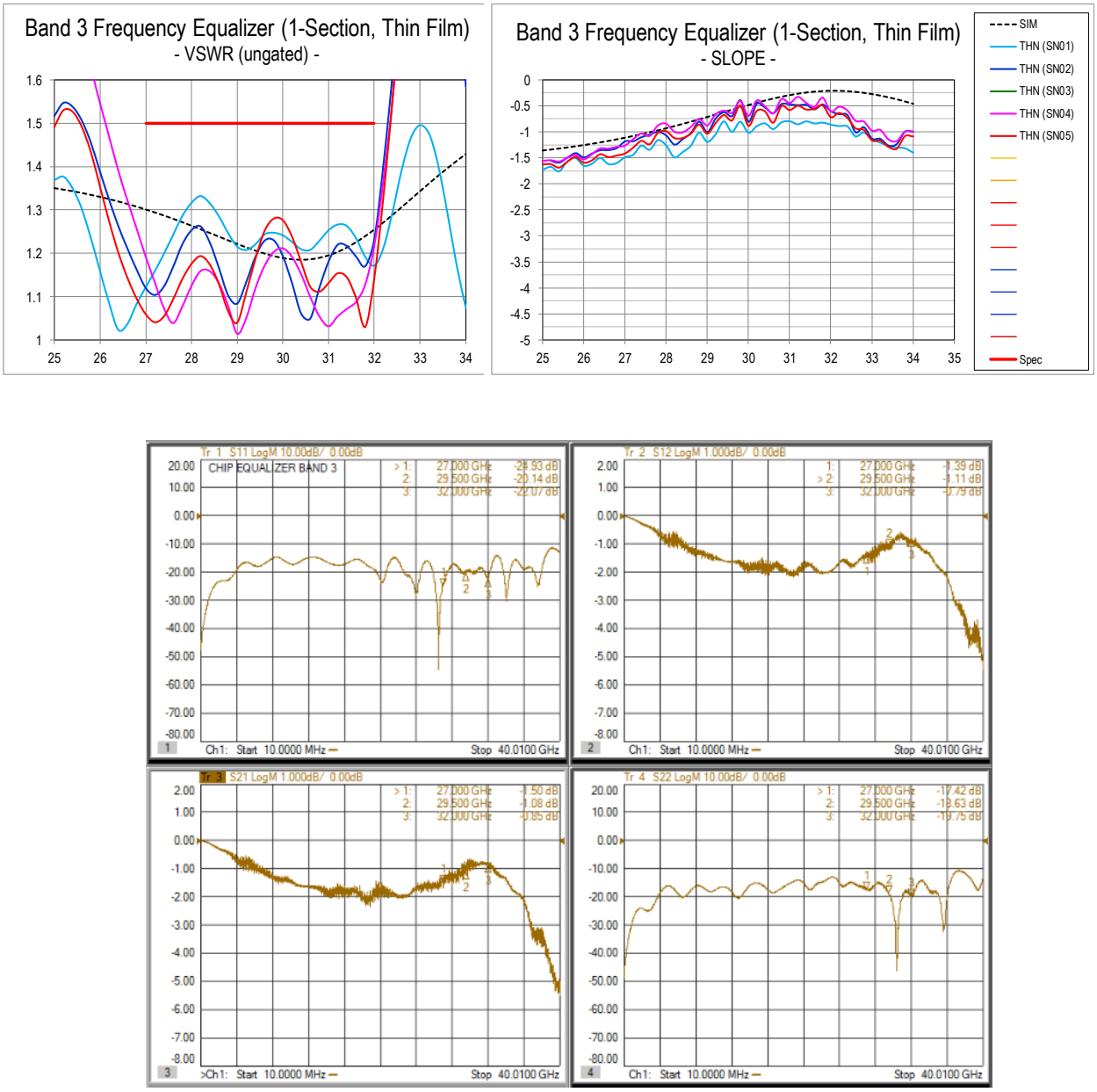

Figure 14. Typical RF performance of CEHF1270P320SMTF: VSWR gated (top left), VSWR ungated (bottom right)

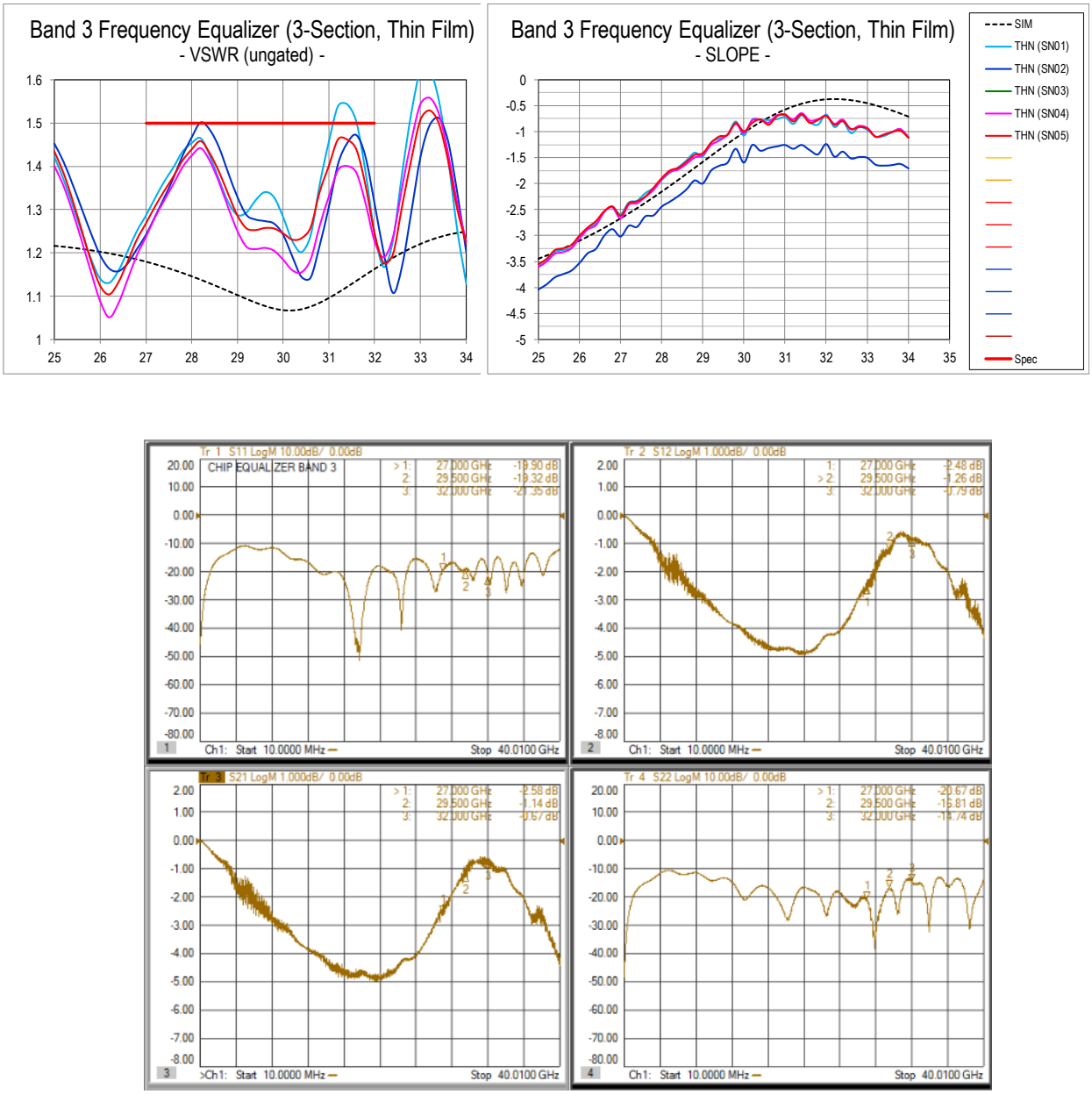

Figure 15. Typical RF performance of CEHF3270P320SMTF: VSWR gated (top left), VSWR ungated (bottom right)

7. Qualification Test

The purpose of this test is to subject the chip equalizers to the conditions as specified in the test plan TP-9279 and qualify them internally for the markets to be served. The flow chart of the qualification has been shown in Figure 20. Five samples of each design will be subjected to the Group A tests. The Specification Control Drawing (SCD, see Tables 1 through 4) of the device is the governing document for all specification limits for each test, with any exceptions noted herein. Qualification testing references MIL-PRF-55342, for Class L devices, with the exceptions noted in this document.
Devices were mounted on destruct fixturing in order to facilitate performance of the required tests. Removable RF connectors were be mounted only when RF test is called out. Test frequencies are defined as 'low' = 1GHz, 'mid' = (maxfreq-1GHz)/2 = 20.5 GHz, rounded to the nearest 2-decimal places, & 'high' = 42 GHz per SCD.
Change in resistance incurred by tests performed was noted (if any) and used for the specification risk assessment and the final device rating. RF performance was verified at the end of each test group.

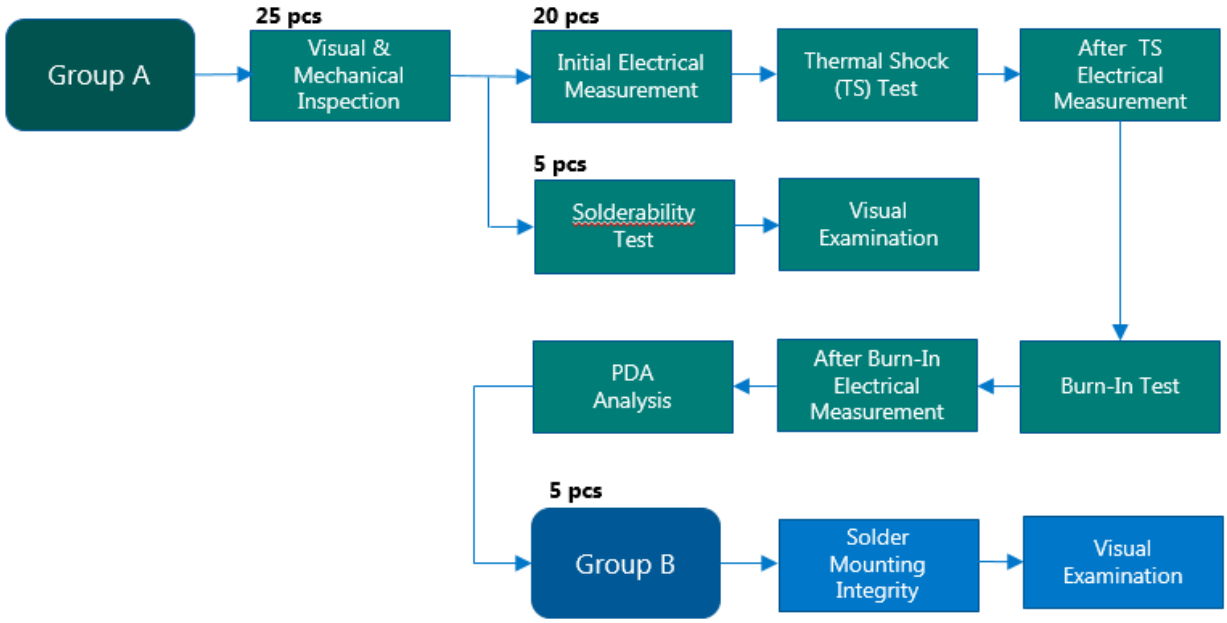

Figure 16. Flowchart of Test Procedure

GROUP A INSPECTION (100% of the lot, 25 samples)

Each inspection lot was subjected to 100% Group A inspection. The inspection lot devices were mounted onto a PCB/test fixture prior to Electrical Inspection.

Visual Mechanical Inspection Results

The materials, design, construction, physical dimensions, markings and workmanship were verified to be in accordance with applicable requirements per the appropriate SCD.

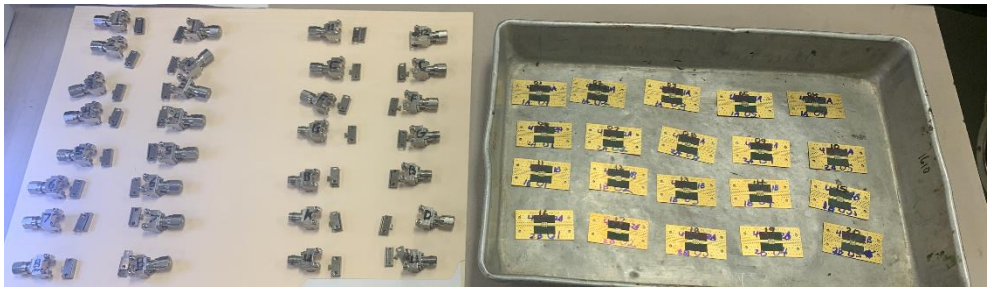

Figure 17. Group A inspection lot (20-piece sample lot to be exposed to thermal and burn-in test): test connectors (left), test boards with the DUTs installed (right)

Initial Electrical (INI) Test Results

VSWR (or Return Loss) has then been measured and recorded at low, mid and high frequencies on a Vector Network Analyzer (VNA), in accordance with MIL-STD-39030, Method 4.6.10. S-parameter file for each device has been captured. Acceptance limits were as per the SCD. The typical RF performance of a Group A sample is shown in Figure 22. As indicated in Table 5, the inspection lot passed the required specification as per SCD.

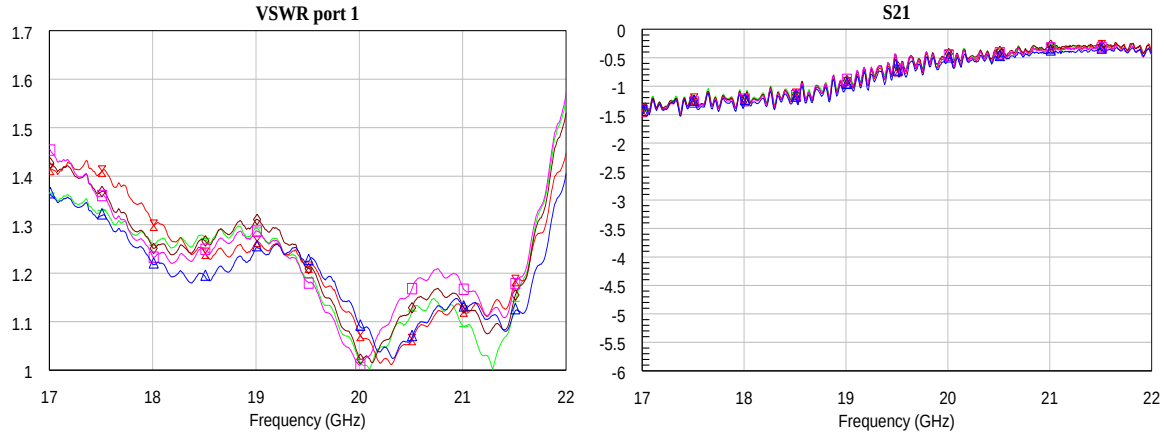

Figure 18. Group A Initial Electrical Test Results – RF performance of a typical sample from the inspection lot (CEHF1170P220SMTF): VSWR (left), insertion loss (right)

Chip Equalizer Qualification Acceptance Testing										
Project / WO:	DD-197206									
Part #:	CEHFx####P###SMTF									
Description:	**C**hip **E**qualizer, **H**igh **F**requency, x = slope in dB, # = Low Freq, **P**ositive slope,									
	# = High Freq, Surface Mount Technology, F = lead free									
Test Plan:	TP-9297									
Test Stage:	2.3.1									
Test Descr:	RF Test (INI)									
Test Equip:	Agilent N5224A VNA (TE91555)									
Operator:	JA									
Start Date	2/15/2020									
End Date	2/15/2020								**Results**	**PASS**
Spec limit:										
VSWR :1										
1.70										
VSWR :1										
Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	1.36	1.46	1.43	1.41	1.37	1.01	1.08	1.10	1.15	1.28
19.5	1.23	1.18	1.21	1.21	1.19	1.45	1.49	1.46	1.63	1.26
22.0	1.41	1.57	1.53	1.45	1.56	1.06	1.16	1.11	1.09	1.34
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	1.21	1.05	1.11	1.19	1.33	1.35	1.29	1.31	1.34	1.21
29.5	1.35	1.23	1.13	1.16	1.07	1.30	1.27	1.23	1.20	1.18
32.0	1.16	1.11	1.29	1.22	1.54	1.12	1.25	1.32	1.08	1.17
IL (dB)										
Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	-1.47	-1.45	-1.42	-1.44	-1.44	-3.82	-3.85	-3.81	-3.91	-3.89
19.5	-0.62	-0.59	-0.52	-0.57	-0.56	-1.55	-1.48	-1.61	-1.70	-1.52
22.0	-0.42	-0.44	-0.38	-0.37	-0.43	-0.49	-0.45	-0.45	-0.79	-0.64
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	-1.32	-1.13	-1.20	-1.15	-1.10	-2.59	-3.01	-2.55	-2.53	-2.55
29.5	-1.04	-0.60	-0.71	-0.53	-0.79	-1.08	-1.67	-1.16	-1.01	-1.08
32.0	-0.80	-0.43	-0.63	-0.42	-0.59	-0.61	-1.21	-0.63	-0.59	-0.60

Table 5. Group A Initial Electrical Test Results - Summary

Thermal Shock

The inspection lot samples were exposed to 10 cycles of thermal shock, -55°C to +125°C in accordance with MIL-STD-202, Method 107 (see Table 6). The equipment used for the test consisted of Thermotron, model ATS-30-4-4 with the asset tag # TE90075.

STEP	TEMPERATURE (°C)	TIME (MINUTES)
1	-55 (+0/-3)	15 min.
2	+25 (+10/-5)	5.0 max.
3	+125 (+3/-0)	15 min.
4	+25 (+10/-5)	5.0 max.

Table 6. Thermal Shock temperature levels and exposure times

After Thermal Shock Electrical (ATS) Test Results

Measure and record VSWR (or Return Loss [RL]) at low, mid and high frequencies on a Vector Network Analyzer (VNA) was measured and recorded, in accordance with MIL-STD-39030, Method 4.6.10. S-parameter files for each device were captured after the loss of the fixture was removed. Acceptance limits: VSWR per the SCD and Insertion Loss Δ ±0.5dB from the previous electrical test at low, mid and high frequencies in the device's frequency band. As indicated in Table 7, the inspection lot samples passed the requirements.

Chip Equalizer Qualification Acceptance Testing

smiths interconnect bringing technology to life

Project / WO:	DD-197206									
Part #:	CEHFx###P###SMTF									
Description:	**C**hip **E**qualizer, **H**igh **F**requency, x = slope in dB, # = Low Freq, **P**ositive slope,									
	# = High Freq, Surface Mount Technology, F = lead free									
Test Plan:	TP-9297									
Test Stage:	2.3.3									
Test Descr:	RF Test Post Thermal Shock (ATS)									
Test Equip:	Agilent N5224A VNA (TE91555)									
Operator:	JA									
Start Date	2/16/2020									
End Date	2/16/2020								**Results**	**PASS**

Spec limit:	
VSWR :1	**Attn Δ (± dB)**
1.70	0.5

VSWR :1 Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	1.36	1.38	1.39	1.37	1.40	1.02	1.08	1.13	1.17	1.23
19.5	1.22	1.23	1.19	1.22	1.21	1.44	1.46	1.46	1.60	1.31
22.0	1.38	1.43	1.58	1.39	1.44	1.05	1.13	1.17	1.09	1.29
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	1.218	1.083	1.244	1.204	1.377	1.347	1.257	1.336	1.331	1.266
29.5	1.376	1.264	1.328	1.215	1.077	1.319	1.323	1.266	1.196	1.243
32.0	1.167	1.134	1.24	1.131	1.496	1.134	1.352	1.293	1.099	1.242

IL (dB) Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	-1.46	-1.42	-1.43	-1.37	-1.38	-3.80	-3.83	-3.83	-3.91	-3.88
19.5	-0.61	-0.61	-0.51	-0.53	-0.54	-1.54	-1.55	-1.63	-1.72	-1.49
22.0	-0.42	-0.46	-0.39	-0.31	-0.40	-0.47	-0.49	-0.53	-0.84	-0.63
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	-1.24	-1.07	-1.17	-1.11	-1.11	-2.56	-2.72	-2.51	-2.54	-2.44
29.5	-0.98	-0.65	-0.83	-0.57	-0.85	-1.00	-1.43	-1.02	-1.02	-1.01
32.0	-0.71	-0.43	-0.66	-0.48	-0.68	-0.57	-0.95	-0.54	-0.59	-0.54

Δ IL (dB) Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	0.00	0.03	-0.01	0.07	0.06	0.02	0.02	-0.02	0.00	0.01
19.5	0.01	-0.02	0.01	0.05	0.01	0.01	-0.08	-0.02	-0.02	0.03
22.0	0.01	-0.03	-0.01	0.06	0.03	0.02	-0.05	-0.08	-0.04	0.00
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	0.08	0.06	0.03	0.04	0.00	0.03	0.30	0.04	0.00	0.11
29.5	0.05	-0.05	-0.11	-0.05	-0.06	0.07	0.25	0.14	-0.01	0.07
32.0	0.10	-0.01	-0.03	-0.05	-0.08	0.04	0.26	0.09	0.01	0.06

Table 7. Group A Post Thermal Shock Electrical Inspection Results

Bake (100% de-rated burn-in):

The devices were subjected to a 168 hour bake (100% de-rated burn-in) at 150°C. The equipment used in the test – Fischer Scientific isotemp oven (# TE91660) and Omega HH502 thermometer (# TE40080). The entire lot was placed in the appropriate burn in fixture for the product family in a temperature controlled preheated chamber. The power was turned on and 168-hour test started. The temperature was monitored periodically to ensure test is not disrupted. After 168 hours had been concluded, the parts were removed from the chamber and stabilized at the room temperature until tray was cool (1 hour min).

After Burn-in Electrical Test Results

VSWR (or Return Loss) has then been measured and recorded at low, mid and high frequencies on a Vector Network Analyzer (VNA), in accordance with MIL-STD-39030, Method 4.6.10. S-parameter file for each device has been captured. Acceptance limits: VSWR per the SCD and Insertion Loss $\Delta \pm 0.5$dB from the previous electrical test at low, mid and high frequencies in the device's frequency band. As shown in Table 8, the inspection lot samples passed the requirements.

Chip Equalizer Qualification Acceptance Testing										
Project / WO:	DD-197206									
Part #:	CEHFx###P###SMTF									
Description:	**C**hip **E**qualizer, **H**igh **F**requency, x = slope in dB, # = Low Freq, **P**ositive slope,									
	# = High Freq, Surface Mount Technology, F = lead free									
Test Plan:	TP-9297									
Test Stage:	2.3.5									
Test Descr:	RF Test Post Bake (ABI)									
Test Equip:	Agilent N5224A VNA (TE91555)									
Operator:	JA									
Start Date	1/24/2020									
End Date	1/27/2020								**Results**	**PASS**
Spec limit:										
VSWR :1	**Attn Δ (± dB)**									
1.70	0.50									
VSWR :1										
Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	1.37	1.38	1.43	1.42	1.42	1.02	1.03	1.10	1.12	1.20
19.5	1.21	1.15	1.19	1.20	1.16	1.37	1.43	1.42	1.58	1.29
22.0	1.51	1.65	1.57	1.52	1.61	1.18	1.09	1.03	1.07	1.16
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	1.23	1.03	1.14	1.15	1.16	1.35	1.31	1.30	1.36	1.32
29.5	1.26	1.21	1.16	1.16	1.10	1.30	1.26	1.25	1.20	1.21
32.0	1.33	1.31	1.46	1.37	1.68	1.13	1.10	1.14	1.11	1.19
***IL (dB)**										
Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	-1.66	-1.65	-1.67	-1.58	-1.58	-3.94	-3.99	-3.99	-4.21	-4.04
19.5	-0.84	-0.83	-0.83	-0.78	-0.74	-1.73	-1.74	-1.83	-2.09	-1.72
22.0	-0.69	-0.72	-0.70	-0.59	-0.63	-0.70	-0.68	-0.69	-1.15	-0.81
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	-1.48	-1.38	-1.35	-1.37	-1.47	-2.73	-3.16	-2.82	-2.88	-2.78
29.5	-1.32	-0.90	-0.97	-0.76	-1.04	-1.27	-1.78	-1.28	-1.44	-1.31
32.0	-1.14	-0.82	-0.93	-0.77	-1.00	-0.77	-1.33	-0.81	-0.98	-0.85
Δ IL (dB)										
Frequency										
(GHz)	**SN01**	**SN02**	**SN03**	**SN04**	**SN05**	**SN11**	**SN12**	**SN13**	**SN14**	**SN15**
17.0	-0.19	-0.22	-0.24	-0.22	-0.20	-0.14	-0.17	-0.16	-0.29	-0.17
19.5	-0.23	-0.21	-0.32	-0.26	-0.20	-0.19	-0.18	-0.20	-0.36	-0.24
22.0	-0.27	-0.26	-0.31	-0.28	-0.23	-0.23	-0.18	-0.16	-0.31	-0.17
	SN06	**SN07**	**SN08**	**SN09**	**SN10**	**SN16**	**SN17**	**SN18**	**SN19**	**SN20**
27.0	-0.24	-0.31	-0.19	-0.26	-0.36	-0.18	-0.44	-0.31	-0.35	-0.34
29.5	-0.34	-0.25	-0.15	-0.19	-0.20	-0.26	-0.35	-0.26	-0.43	-0.30
32.0	-0.43	-0.39	-0.27	-0.29	-0.32	-0.21	-0.38	-0.27	-0.39	-0.31

Table 8. Group A Post Burn In Electrical Test Results - Summary

Percent Defective Allowable (PDA) Analysis Results

Percentage Defective Allowable (PDA) Analysis was performed on the Group A inspection lot. The defective percentage was calculated to be 0% which is below an acceptable 10%. It was concluded that the inspection lot that was subjected to the test passed the Group A testing and could be moved over to the Group B test stage.

GROUP B INSPECTION (5 samples):

Five (5) samples from the Group A inspection lot were randomly selected. Devices were soldered to the suitable substrate. A .75-kilogram force was applied chip edge for 30 seconds per MIL-PRF-55342,

Method 4.8.13.1. After the test, the devices were inspected for any evidence of mechanical damage. No damage was observed The DUTs passed the test.

Chip Equalizer Qualification Acceptance Testing smiths interconnect bringing technology to life										
Project / WO:	DD-197206									
Part #:	CEHFx###P###SMTF									
Description:	**C**hip **E**qualizer, **H**igh **F**requency, x = slope in dB, # = Low Freq, **P**ositive slope,									
	# = High Freq, Surface Mount Technology, F = lead free									
Test Plan:	TP-9297									
Test Stage:	3.1.1									
Test Descr:	Solder Mounting Integrity									
Test Equip:	Chatillon Force Gauge									
Operator:	BS									
Start Date	1/27/2020									
End Date	1/27/2020									
Spec limit:										
Force (kg.)	**Time (secs)**									
2.0	30									
SN	**Result**									
21	Pass									
22	Pass									
23	Pass									
24	Pass									
25	Pass									

Table 9. Group B Test Results - Summary

8. Qualification Test – Summary and Conclusion

The high frequency chip equalizer product line at this point consists of four products – CEHF1170P220SMTF (17 – 22 GHz, 1 dB slope), CEHF3170P220SMTF (17 – 22 GHz, 3 dB slope), CEHF1270P320SMTF (27 – 32 GHz, 1 dB slope), and CEHF3270P320SMTF (27 – 32 GHz, 3 dB slope). Samples of all four chip equalizers above have been electrically and thermally tested; the test results presented in this test report are evidence of the performance that meets the required specifications.

A rigorous qualification testing as per TP-9279 has also been performed on a 25-piece inspection lot of the four above designs. The test consisted of Group A and Group B testing; the devices were subjected to thermal shock, burn in test, and solder mount integrity test. The results of these qualification tests have been presented in this report. As shown, the inspection lot passed all the specifications as required by the TP-9279 and corresponding SCD. It has therefore been determined that the products **CEHF1170P220SMTF, CEHF3170P220SMTF, CEHF1270P320SMTF, and CEHF3270P320SMTF are qualified to be released into a full production**.