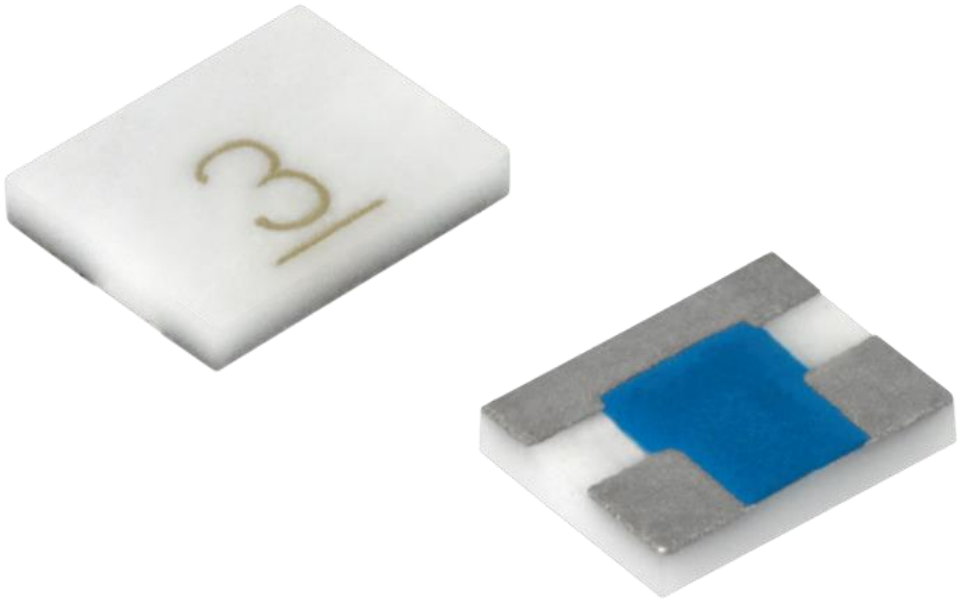
smiths interconnect
bringing technology to life

Power Handling Test Report

TS05XX Series Attenuators
High Power Qualification Test

Walter McKinley,
Juan Ayala, 10/19/2018



1. Scope

The purpose of this report is qualify the power handling capability of the TS05XX product line. This report describes the test procedure and presents test results to support qualification. The power is supplied using DC (Direct Current) power to provide maximum heat for the device's internal resistors on a destruct type Printed Circuit Board (PCB). Electrical tests are completed by measuring DC Resistance (DCR) and Calculating DC Attenuation (DCA). A batch of 4 different attenuation chips with 4 samples in each batch is studied. The Group A test is thermal shock, followed by an 168 hour burn-in of which at least half of the total burn-in time is at a temperature of 100 C. Then the same chip goes to a Group B test consisting of a Short Term Overload (STOL). The change is DCA is recorded after each step. The cumulative change in DCA is analyzed to determine the part's power handling qualification.

Thermal Finite Element Analysis (FEA) simulations are performed to calculate the maximum power handling of the family of parts. The simulations are calculated for chips with attenuation values from 1dB to 20dB in 1 dB increments. The results are used to correlate physical testing of a selected range of attenuation values to evaluate the power rating of the entire TS05 value of attenuation values.

The motivation for this report came from Project DD-205897 to qualify the power handling capabilities of the TS05XX product line used in multiple programs for customer Raytheon Missile Systems.

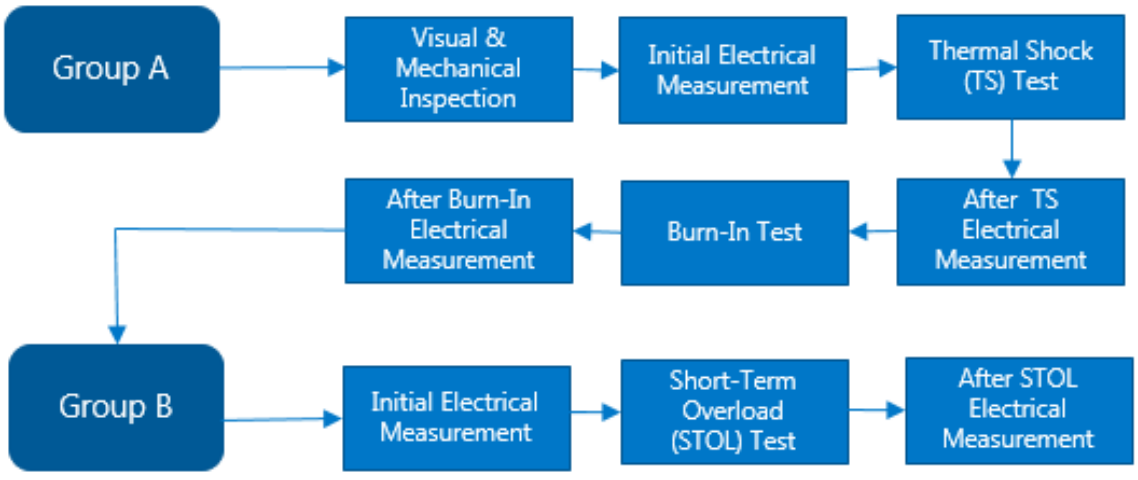


Figure 1 – Flowchart of Test Procedure

2. Specifications

The TS05XX series is offered as a planar, single wrap, triple wrap or wire bondable version. The series has attenuation values between 0 to 20 in 1dB increments. Both a RoHS and non-RoHS version is offered.

Nominal Impedance: 50Ω
Frequency Range: DC-18GHz

Attenuation Accuracy				
Attenuation (dB)	DC - 4 GHz	4-8 GHz	8 - 12.4 GHz	12.4 - 18 GHz
0	-0, + 0.3	-0, +0.5	-0, +0.5	-0, +0.5
1 - 3	+/- 0.3	+/- 0.5	+/- 0.5	+/- 0.5
4 - 6	+/- 0.4	+/- 0.5	+/- 0.5	+/- 0.75
7 - 10	+/- 0.5	+/- 0.5	+/- 0.75	+/- 1.0
11 - 15	+/- 0.75	+0.5, -3.0	+0.5, -3.5	---
16 - 20	+/- 1.0	+0.5, -4.0	+1.0, -6.0	---

Table 1 – Attenuation Accuracy

VSWR	
Frequency Range	VSWR
DC - 4 GHz	1.25 MAX
4 - 8 GHz	1.35 MAX
8 - 18 GHz	1.50 MAX

Table 2 - VSWR

Input Power CW	
Attenuation	Power
(dB)	(W)
0 - 1	4.00
2 - 3	2.00
4 - 10	1.00
11 - 20	0.75
Full Rated Power at 100 C. Power is derated linearly to 0 Watts at 150 C	

Table 3 - Input Power CW

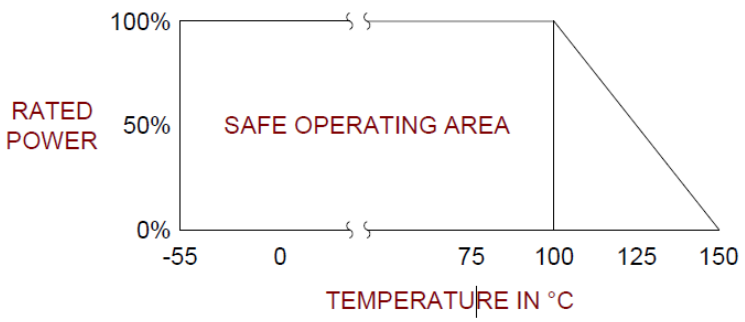


Figure 2 – Power Derating at Temperature. Power is linearly derated to 0 W at 150 C

3. Test Description

The attenuator family shall be divided into four (4) power handling test groups. Each power handling group will have one attenuation value tested to qualify the group. Preferred Attenuation values: 1dB, 3dB, 10dB & 20dB were tested. Attenuation values in each power group are noted in the Specifications section and also in the appropriate Specification Control Drawing (SCD) of the attenuator family. The Internal Qualification Inspection performed is listed in TP-9251.

4. Test Procedure

Group A: Each inspection lot shall be subjected to 100% Group A Inspection for all attenuation values. Devices must be mounted to a PCB prior to Electrical Inspection.

Visual / Mechanical Inspection: All devices Verify that materials, design, construction, physical dimensions, markings and workmanship are in accordance with applicable requirements per the appropriate SCD.

Initial (INI) Electrical: Measure and record DC resistance between I/O path and from each I/O port to Ground paths in accordance with MIL-STD-202, Method 303. Calculate DC Attenuation. Acceptance limits shown in the specifications section or SCD.

Thermal Shock: Subject attenuators to 10 cycles of thermal shock, -55°C to +125°C in accordance with MIL-STD-202, Method 107. See Table 1:

Table 4 - Thermal Shock requirements listed in TP-9251

STEP	TEMPERATURE (°C)	TIME (MINUTES)
1	-55 (+0/-3)	15 min.
2	+25 (+10/-5)	5.0 max.
3	+125 (+3/-0)	15 min.
4	+25 (+10/-5)	5.0 max.

After Thermal Shock (ATS) Electrical: Measure and record DC resistance between I/O path and from each I/O port to Ground paths in accordance with MIL-STD-202, Method 303. Calculate DC Attenuation. Acceptance limits shown in the specifications section or SCD. All DCA measurements must be within ±.2dB of the INI DCA measurements.

Burn In: Burn-in properly mounted and terminated devices in increasing DC power and base temperature steps until the maximum power for each test group (attenuation value) and 100°C base temp is achieved. The entire test duration must be 168 hours minimum with at least half of the test period at the maximum temperature and power specified in the SCD. Record and Report the power, temperature and duration for each step.

After Burn-In (ABI) Electrical: Measure and record DC resistance between I/O path and from each I/O port to Ground paths in accordance with MIL-STD-202, Method 303. Calculate DC Attenuation. Acceptance limits shown in the specifications section or SCD. All DCA measurements must be within ±.2dB of the INI DCA measurements.

Group B: Group B inspection shall be samples that have been subjected to Group A Inspection.

Initial (INI) Electrical: Measure and record DC resistance between I/O path and from each I/O port to Ground paths in accordance with MIL-STD-202, Method 303. Calculate DC Attenuation. Acceptance limits shown in the specifications section or SCD. Previous test final measurement results may be used.

Short-Term Overload: Apply 2.5 times the maximum working voltage (not to exceed twice the maximum rated voltage) for duration of five (5) seconds to devices mechanically mounted on a suitable heat sink. There shall be no evidence of arcing, burning, or charring.

After Short-Term Overload (ASTOL) Electrical: Measure and record DC resistance between I/O path and from each I/O port to Ground paths in accordance with MIL-STD-

202, Method 303. Calculate DC Attenuation. Acceptance limits shown in the specifications section or SCD.

5. Results

The change in attenuation was measured for each of the 4 samples at each of the 4 attenuation values yielding a total of 16 measurements. The change is attenuation for each sample after each test is shown below in Table 5. A graphical representation showing average change in attenuation for a 4 unit sample size at each attenuation value is shown in Figure 3. The bar graph shows the average of each of the 4 samples along with error bars showing one standard deviation. The upper and lower limits at +0.2 dB and -0.2 dB on the chart represent the acceptable limits of variation of attenuation for the qualification test.

The majority of attenuation change at each attenuation value occurs after the Short Term Overload (STOL). This test is expected to cause the most amount of damage to the attenuator. Historically, most parts that pass through qualification fail during the STOL test. The Thermal Shock test causes the negligible change in attenuation on all 4 attenuation values. The Burn-In Test shows some change in attenuation for the 1dB sample with negligible amount of change for the remaining samples.

The acceptance limits of the test is a +/- 0.2 dB change in attenuation value. The maximum change in attenuation of tested samples occurs in the 20dB sample. The change in attenuation does not exceed +/- 0.02 dB, or 10% of the allowable attenuation shift. The standard deviation of the 20dB sample is 0.03 dB. So, 99.7% confidence interval for the worst case test shows a change in attenuation of +/- 0.11 dB. This is approximately half as much as the acceptance criteria for the qualification test.

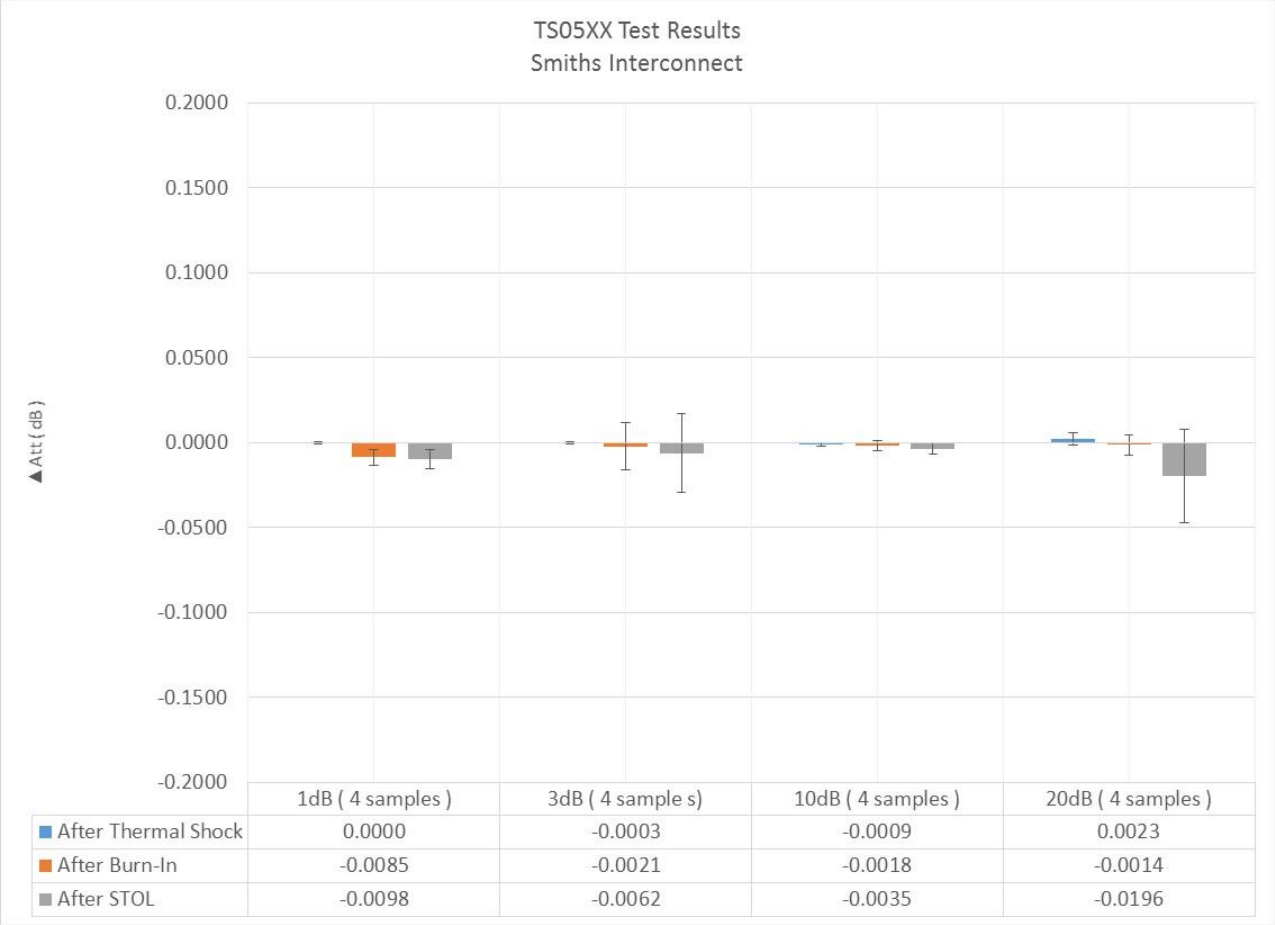


Figure 3 – Graphical Results of TS05XX Test

	Initial Electrical	Thermal Shock		Final Burn In		STOL	
	Att (dB)	Att (dB)	▲Att (dB)	Att (dB)	▲Att (dB)	Att (dB)	▲Att (dB)
SI_1dB_01	1.0033	1.0031	-0.0002	0.9881	-0.0152	0.9850	-0.0183
SI_1dB_02	0.9831	0.9830	-0.0001	0.9777	-0.0054	0.9771	-0.0060
SI_1dB_03	0.9829	0.9835	0.0007	0.9770	-0.0059	0.9764	-0.0065
SI_1dB_05	0.9859	0.9854	-0.0005	0.9784	-0.0075	0.9776	-0.0083
SI_3dB_01	2.9907	2.9913	0.0006	2.9925	0.0018	2.9905	-0.0002
SI_3dB_02	2.9925	2.9922	-0.0003	3.0055	0.0130	2.9734	-0.0190
SI_3dB_04	3.0110	3.0107	-0.0003	3.0076	-0.0034	3.0345	0.0235
SI_3dB_05	2.9764	2.9754	-0.0010	2.9565	-0.0199	2.9472	-0.0292
SI_10dB_01	10.0990	10.0987	-0.0002	10.1009	0.0019	10.0993	0.0003
SI_10dB_02	10.1198	10.1189	-0.0009	10.1160	-0.0037	10.1117	-0.0080
SI_10dB_03	10.1133	10.1129	-0.0004	10.1120	-0.0013	10.1104	-0.0029
SI_10dB_04	10.1273	10.1251	-0.0022	10.1232	-0.0041	10.1238	-0.0035
SI_20dB_01	20.4608	20.4580	-0.0029	20.4595	-0.0013	20.4009	-0.0600
SI_20dB_02	20.1827	20.1871	0.0044	20.1800	-0.0027	20.1782	-0.0045
SI_20dB_03	19.8389	19.8432	0.0043	19.8451	0.0062	19.8401	0.0012
SI_20dB_05	20.5038	20.5072	0.0034	20.4961	-0.0077	20.4888	-0.0150

Table 5 – Test Results showing total change in attenuation.

TS05XX - Test Results: Change in Attenuation						
	After Thermal Shock		After Burn-In		After STOL	
	AVG	STDEV	AVG	STDEV	AVG	STDEV
1dB (4 samples)	0.0000	0.0005	-0.0085	0.0046	-0.0098	0.0058
3dB (4 sample s)	-0.0003	0.0006	-0.0021	0.0137	-0.0062	0.0232
10dB (4 samples)	-0.0009	0.0009	-0.0018	0.0028	-0.0035	0.0034
20dB (4 samples)	0.0023	0.0035	-0.0014	0.0058	-0.0196	0.0278

Table 6 – Test Results showing average and standard deviation of change in attenuation

6. Simulation

Thermal Finite Element Analysis (FEA) simulations are performed to calculate the maximum power handling of the family of parts. The simulations are calculated for chips with attenuation values from 1dB to 20dB in 1 dB increments. The results are used to correlate physical testing of a selected range of attenuation values to evaluate the power rating of the entire TS05 value of attenuation values.

The simulations model includes the attenuator PCB, fixture board and the heatsink. The simulation takes into account conduction heat transfer into the heat sink and free convection transfer into the ambient surroundings. The base of the heatsink is set to an isothermal boundary at 100 C. The results of the simulation show the amount of power required to heat any point on the film to 150 C. The film temperature of 150 C is chosen as a conservative design point to avoid the possibility of resistance drift due to thermal coefficient of resistivity (TCR). Significantly higher film temperature can lead to an expected drift in resistance and corresponding change in attenuation.

The results of the simulation are shown below. The Table also contains the attenuation values that of the burn-in test along with the final part power rating. The results of the simulation and the burn-in power test show the real world power handling of the part. Following industry standards, the power rating of the attenuator is described as the maximum possible power under ideal circumstances mounted onto an “infinite” heatsink. The true power handling of the part will need to be reduced, or “derated”, to account for finite thermal conductivity of PCB, solder and thermal grease.

TS05xx Power Rating			
Attenuation (db)	Simulated Power Handling (W)	Burn-In Test Power (W)	Power Rating (W)
1	4.32	4	5
2	2.381	-	2
3	1.613	2	2
4	1.316	-	1
5	1.262	-	1
6	1.174	-	1
7	1.153	-	1
8	1.121	-	1
9	1.051	-	1
10	1.003	1	1
11	0.959	-	0.75
12	0.918	-	0.75
13	0.903	-	0.75
14	0.874	-	0.75
15	0.851	-	0.75
16	0.823	-	0.75
17	0.724	-	0.75
18	0.709	-	0.75
19	0.697	-	0.75
20	0.686	0.75	0.75

Table 7 – Results of Thermal FEA

7. Conclusion

Based on the testing conducted, the TS05XX Attenuator product line will successfully meet the power ratings described in the specification section.
The revised power rating for the 0 to 1 dB is 5.00 W, the 2 to 3 dB is 2 W, the 4 to 10 dB is 1 W and the 11 to 20 dB is 0.75 Watts.