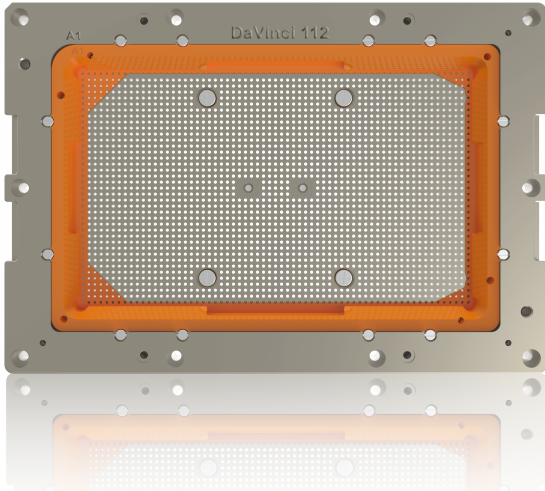


DaVinci 112 Test Socket

The Next Generation of High Speed Test Solutions



The DaVinci 112 test socket extends the 'DaVinci' Series with an innovative solution for testing the most complex functionality of ASICs (Application Specific Integrated Circuits).

These new systems have increased processing power by 5000 times and the current products can reach 5 petaFLOPS of bandwidth.

Addressing high speed signaling, device complexity and power requirements is leading to the largest Integrated Circuits ever manufactured, with pin count well over 4000 I/O's all working in tandem to meet the specification.

Testing these devices at full functionality is challenging. With hundreds of PAM-4 signals, the ability to isolate pin-to-pin cross-talk at the fundamental frequency below -40dB becomes critical.

The DaVinci 112 increases production yields and throughput, eliminating false faults and complete functional failures.

*PetaFLOPS and teraFLOPS are immense measures of processing speed. One petaFLOPS is equal to one thousand teraFLOPS.

DaVinci 112 offers significant improvement of the cross-talk isolation over DaVinci 56

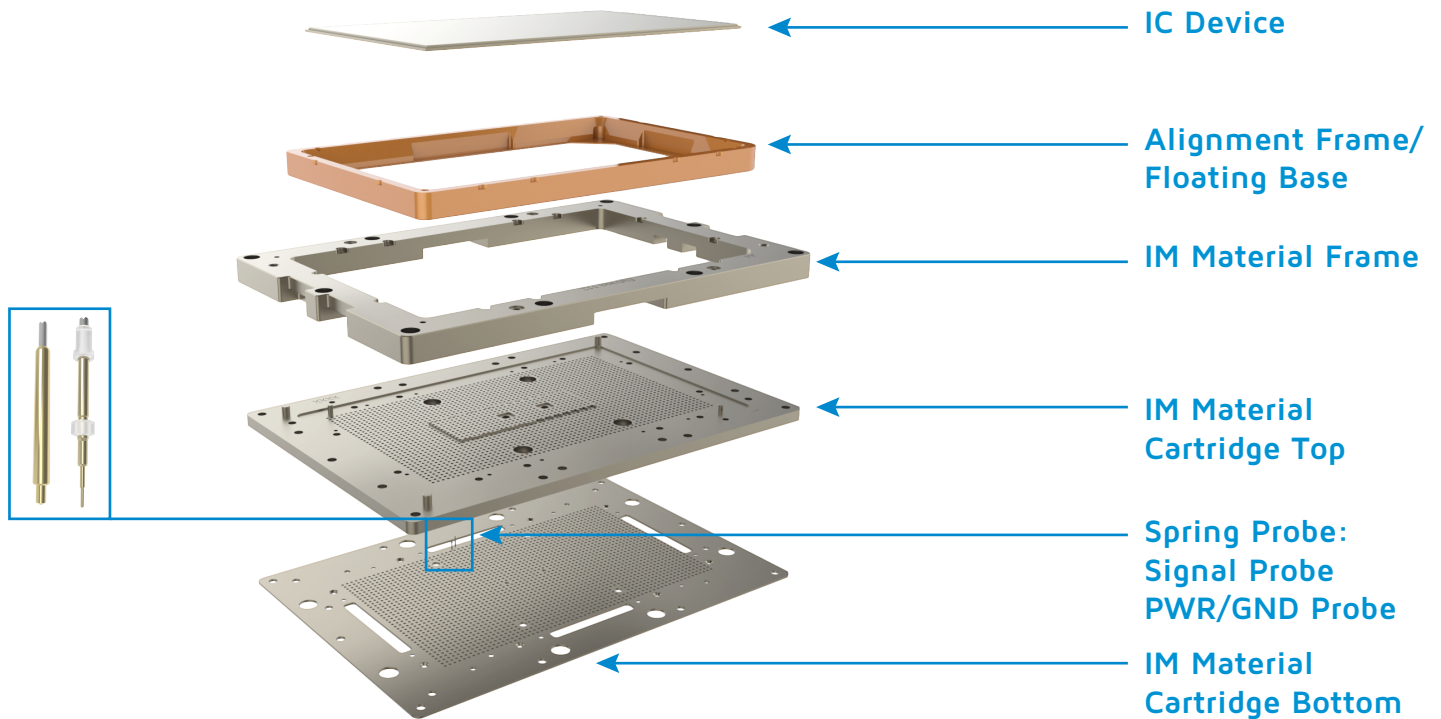
Value proposition

- Designed for devices $\geq 70 \text{ mm}^2$ and over 4000 inputs/outputs and coplanarity tolerance of up to $\pm 0.65 \text{ mm}$
- New ground probe design for cleaner power delivery and improved noise isolation
- Increased spring probe travel (0.8mm) to accommodate large device co-planarity tolerances
- Protection against socket deflection caused by large number of spring probes

End Product Markets

- Wired Communication
- High Performance Computing
- Automotive
- Data Centers
- AI & Deep Learning

Product Structure



Product Features

- Solution for BGA, LGA and other variants
- Spring probe technology using Homogenous Alloy gold plated
- Short signal path 4.90 mm test height
- 43, 50 Ohm impedance (single ended)
- RF Bandwidth up to 40 GHz @ -1dB IL
- Consistent stable contact resistance 80 mΩ (Ave)
- Tri-Temp socket design to support -55 °C to +125 °C
- Designed for manual test, bench test, and HVM production test using the same socket
- GND block design configurable for System Impedance

Benefits

- Long contact life, tested to 500K insertions
- Excellent DC performance
- Impedance can match system or defined as needed
- RF Bandwidth up to 40 GHz @ -1dB IL
- Patented Insulated Metal socket housing for optimal signal integrity performance and strength
- Precision-machined socket housing ensures robust mechanical performance
- Field repairable, replace a single probe or full array without the need for additional training
- Cleaning and repair can be done without taking production equipment offline
- Match existing PCB socket footprint and test hardware lead to cost saving for customers

Technical Characteristics

	DaVinci 45G		DaVinci 56	DaVinci 112
Mechanical & Environmental				
Minimum Pitch	>0.7mm	0.65mm	0.8mm*	0.8mm*
Compliance / Travel	0.50mm	0.40mm	0.50mm	0.8mm
Operating Temperature	-55° to +125°C		-55° to +125°C	-55° to +125°C
Life Span	500,000 cycles		500,000 cycles	500,000 cycles
Electrical				
Loop Inductance	0.71 nH		0.57 nH	0.89 nH
Mutual Capacitance	0.73 pF		0.68 pF	1.19 pF
Contact Resistance	80 mΩ		<80 mΩ	<80 mΩ
Current Carrying Capacity	3.0 A		3.0 A	3.7 A
Bandwidth (-1dB)	45 GHz / 26 Gbps		67 GHz / 56 Gbps	67 GHz / 112 Gbps

IM Mechanical Performance

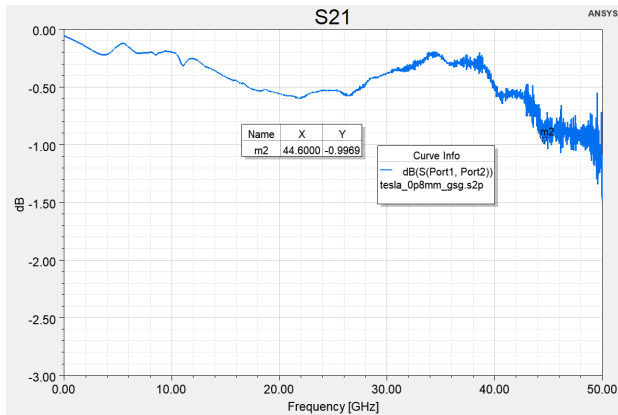
- Proprietary insulated IM Material exhibits least deflection as illustrated by below Max Deflection rates.

Material Type	IM Material	Peak Ceramic	MDS-100
DaVinci 45G 1745 pin BGA	0.009mm	0.085mm	0.046mm
DaVinci 56 4096 pin BGA	0.050mm	0.210mm	0.168mm
DaVinci 112 4096 pin BGA	0.050mm	0.210mm	0.168mm

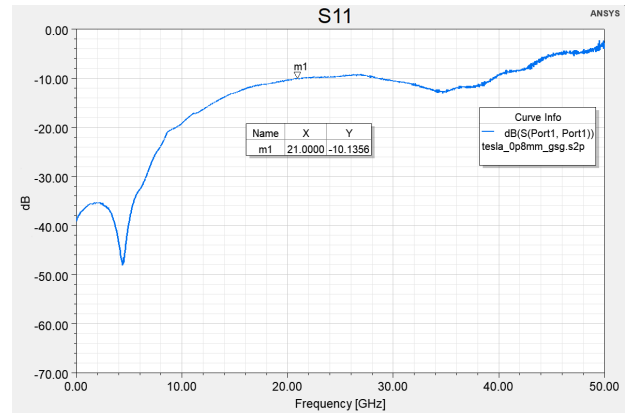
Bandwidth & Frequency Measured Data

DaVinci 45G Single Ended 0.8mm pitch probes - 8A Pattern (3x3 Array)

Insertion Loss

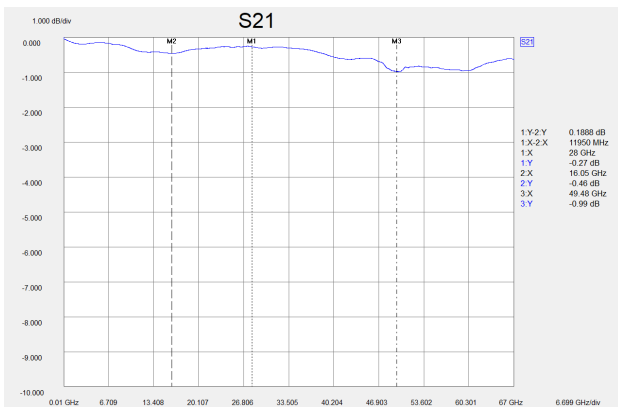


Return Loss

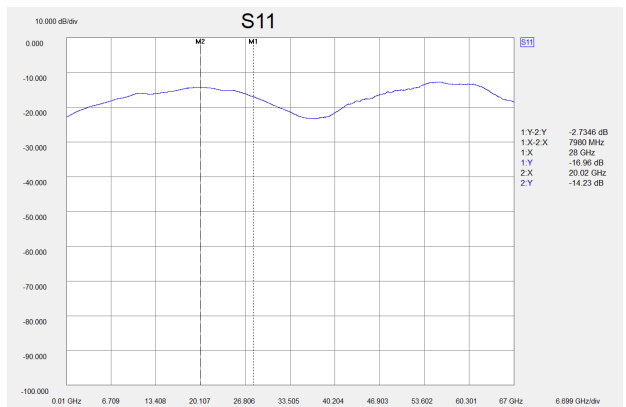


DaVinci 56 Single Ended 0.8mm pitch probes - 8A Pattern (3x3 Array)

Insertion Loss

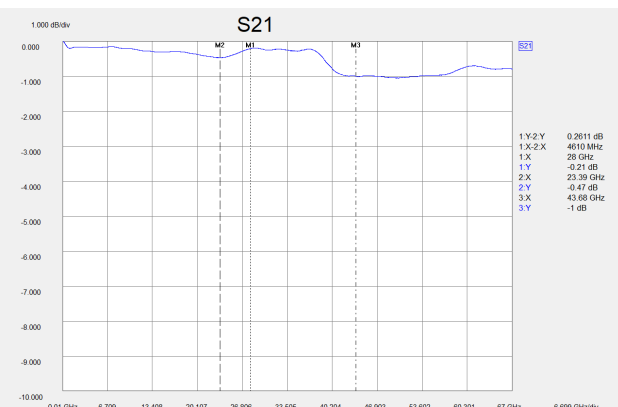


Return Loss



DaVinci 112 Single Ended 0.8mm pitch probes - 8A Pattern (3x3 Array)

Insertion Loss



Return Loss

